OPERATOR'S,ORGANIZATIONAL, DIRECT SUPPORT, GENERAL SUPPORT, AND DEPOT MAINTENANCE MANUAL INCLUDING REPAIR PARTS AND SPECIAL TOOLS LISTS

READER, PUNCHED CARD

RP-152/G

This copy is a reprint which includes current pages from Changes 1 through 8.

## WARNING

## DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT

Be careful when working anywhere within the inclosure of this equipment. Serious injury or death may result from contact with high voltage terminals.

DON'T TAKE CHANCES!

TECHNICAL MANUAL No. 11-7440-215-15 NAVSHIPS 0967-324-0020, TECHNICAL ORDER TO 31W4-2G-31

DEPARTMENTS OF THE ARMY,
THE NAVY AND THE AIR FORCE
WASHINGTON, DC, 16 December 1968

# Operator's, Organizational, Direct Support, General Support, and Depot Maintenance Manual Including Repair Parts and Special Tools Lists READER, PUNCHED CARD RP-152/G <br> (NSN 7040-00-998-0046) 

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## RECORD OF CHANGES

| CHANGE NO. | DATE | TITLE OR BRIEF <br> DESCRIPTION | ENTERED BY |
| :--- | :---: | :---: | :---: |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |



Figure 1-1. Reader, Punched Card RP-152/G, less running spares.

## CHAPTER 1

## INTRODUCTION

## Section I. GENERAL

## 1-1. Scope

This manual describes Reader, Punched Card RP152/G (card reader) (fig. 1-1) and contains operation and maintenance information. It also covers detailed functioning of the card reader and includes the maintenance allocation chart (app. C). Refer to TM 11-7440-239-15/TO 31W4-4-11/NAVSHIPS 0967-324-0110 for installation and checkout procedures.

## 1-2. Indexes of Publications

a. DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.
b. DA Pam 310-7. Refer to DA Pam 310-7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

## 1-3. Forms and Records

a. Reports of Maintenance and Unsatisfactory Equipment. Maintenance forms, records, and reports which are to be used by maintenance personnel at all maintenance levels are listed in and prescribed by TM 38-750 (Army). Air Force personnel will use AFM 66-1 for maintenance reporting and TO-00-35D54 for unsatisfactory equipment reporting. Navy personnel will report maintenance performed utilizing the Maintenance Data Collection Subsystem (MDCS) IAW OPNAVINST 4790.2, Vol 3 and unsatisfactory material/conditions (UR submissions) IAW OPNAVINST 4790.2, Vol 2, chapter 17.
b. Report of Packaging and Handing Deficiencies. Fill out and forward DD Form 6 (Packaging

Improvement Report) as prescribed in AR 700-58/ NAVSUPINST 4030.29/AFR 71-13/MCO P4030.29A, and DSAR 4145.8.
c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 5538/NAVSUPINST 4610.33A/ AFR 75-18/MCO P4610.19B and DSAR 4500.15.

## 1-3.1. Reporting of Errors

The reporting of errors, omissions, and recommendations for improving this publication by the individual user is encouraged. Reports should be submitted on DA Form 2028 (Recommended Changes to Publications and Blank Forms), and forwarded direct to Commander, US Army Electronics Command, ATTN: DRSEL-MA-Q, Fort Monmouth, NJ 07703 (Army); USAFLC Form 252 (Request for TO Revision or Change) and forward direct to prime ALC/MST (Air Force); or forward to: Commander, Naval Electronics Systems Command, Code 4903, Washington, D.C. 20360 (Navy).

## 1-3.2. Administrative Storage

For procedures, forms, and records, and inspections required during administrative storage of this equipment, refer to TM 740-90-1.

## 1-3.3. Destruction of Electronic Materiel

Demolition and destruction of electronic equipment will be under the direction of the commander and in accordance with TM 750-244-2.

## Section II. DESCRIPTION AND DATA

## 1-4. Purpose and Use

a. The card reader is used as an input device component of Digital Subscriber Terminal Equipment (DSTE) sets in the Automatic Digital Network (AUTODIN) military communications system. It reads
perforations in punched cards to establish the information in electrical form and transmits the data to the common control unit (CCU) component of the DSTE set (fig. 1-2).
b. The cards used are Electronic Industries Association (EIA) standard 80 -column cards punched with rectangular holes. The punched data is in the 12bit FIPS-14 code arranged in 80 columns with each column representing a character. The card reader checks that the punched data represents valid characters, then converts the data to the eight-bit American Standard Code for Information Interchange (ASCII). The eight-bit ASCH data (seven data bits and a parity bit) is transferred to the CCU on eight parallel lines at a minimum rate of 150 characters per second.
c. Cards are picked and read by the card reader in response to control signals from the CCU. Protective circuits in the card reader stop the reading in case of any one of eight alarm conditions. For testing and maintenance, the card reader can be operated off-line, independent of the CCU.
1-5. Technical Characteristics of Card Reader
Type of card.............. EIA standard 80-column cards
punched with rectangular
holes.


Figure 1-2. Typical system application, block diagram.

1-6. Items Comprising an Operable Equipment

| NSN Qty |  | Nomenclature, part No., and mfr code | Dimensions (in.) |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Weight (lb) | Depth | Width | Height | Fig. No |
|  |  | NOTE <br> The part number is followed by the applicable 5 -digit Federal supply code for manufacturers, (FSCM) identified in SB 708-42 and used to identify manufacturer, distributor, or Government agency, etc. |  |  |  |  |  |
| 7440-00-998-0046 | 1 | Reader, Punched Card RP-152/G; 58189. A64400-002 | 290 | 30 | 35 | 64 | 1-1 |

## 1-7. Common Names

The following list provides the reference designation, official name, common name, and part number of items frequently mentioned in this manual. Although the full reference designations are shown below, abbreviated
reference designations are frequently used in this manual. Prefix the abbreviated reference designation with the applicable assembly or subassembly identification.

| Reference designation | Item name Reader, Punched Card RP-152/G. | Common name Card reader ...... | Manufacturers part No. <br> ...... A64400-002 |
| :---: | :---: | :---: | :---: |
| A1 | Logic assembly... | Logic assembly. | A64434-001 |
| A2 | Mechanism assembly | Card reader mechanism . | A64421-001 |
| A3 | Control panel. | Control panel. | A64403-001 |
| PS | Power supply ... | .Power supply. | 810003-103 |
| FL1 | Filter assembly | Filter. | A64008-001 |
| B1 | Blower . | . Blower | SM-6-546250 |
| A1A1 | PC card | Solenoid driver | A65209-002 |
| A1A3 | PC card | Lamp driver | SM546659-001 |


| Reference designation | Item name | Common name Manufacturers <br> part No.  |
| :---: | :---: | :---: |
| A1A4 | PC card | .Interface control .......................A65215-001 or A65223-001 |
| A1A5 | PC card. | .Polar interface .........................A65205-001 or A65227-001 |
| A1A6 | PC card. | .Photocell amplifier....................................... A52630-001 |
| A1A7 | PC card | .Data register............................................... A65145-001 |
| A1A8 | PC card | .Invalid character detector .............................. A52634-001 |
| A1A9 | PC card. | .Decode matrix ............................................ A53725-001 |
| A1A10 | PC card. | .Encode matrix ............................................. A53721-001 |
| A1A11 | PC card. | .Decode matrix ............................................ A53725-001 |
| A1A12 | PC card | .Encode matrix ............................................. A53721-001 |
| A1A13 | PC card. | .ASCII encoder............................................. A52622-001 |
| A1A14 | PC card. | .Timing generator ......................................... A65173-001 |
| A1A15 | PC card. | .Timer ........................................................ A65153-001 |
| A1A16 | PC card. | .Control ....................................................... A65141-001 |
| PS1A1 | Circuit card assembly | .+4.75-volt regulator ............................................................................. 3864 |
| PS1A2 | Circuit card assembly ..... | . 12 volt and -12 volt regulators ............................... 38869 |
| PS1A3 | Circuit card assembly ... | -48 volt regulator ................................................. 38874 |
| PS1A12 | Sequence module assembly | Sequence module .................................................. 38982 |

## CHAPTER 2

## OPERATING INSTRUCTIONS

| 2-1. Operator <br> fig. 2-1) | Indicators |
| :---: | :---: |
| Control or indicator | Function |
| AC POWER switch indicator (Z2). | Controls and indicates (white) when ac power is applied. |
| DC POWER indicator (DS1). | Lights (white) when all dc voltages are present in card reader. |
| OUT OF SYN indicator (DS6). | Lights (red) when card reader is out of sync with CCU. |
| PHOTOCELL CHECK indicator (DS4). | Lights (red) when either a card is improperly positioned or a photocell lamp is either dirty or defective. |
| INVALID CHARACTER indicator (DS3). | Lights (red) when a character is either invalid or is not contained in list of permissible characters. |
| CARD ALARM indicator (DS7) | In local test mode, lights (red) when either a hopper empty or stacker full condition is detected. In on-line operation lights when a stacker full condition is detected before end of message has been acknowledged by CCU. |
| CARD JAM indicator (DS5). | Lights (red) when card does not pass through read station within allowable time. |
| PICK FAIL indicator (DS8). | Lights (red) when card is not picked from hopper within allowable time. |
| CANCEL indicator (DS2). | Lights (red) when cancel signal Is received from CCU. |
| NOT ASSIGNED indicator (DS9). | Lights (amber) when card <br> Reader is not assigned at CCU. |
| LAMP TEST switch (Z3). | Lights all indicators, except AC POWER and DC POWER indicators. |
| SINGLE FEED switch-indicator (Z4). | When momentarily pressed, inindicates (white) momentarily and initiates reading of one card |
| AUDIBLE RESET switch (Z1). | After card reader malfunction, press AUDIBLE RESET switch to remove audible alarm at the CCU. |
| START switch-indicator (Z7). | When momentarily depressed, allows cards to be picked for reading in assigned mode under control of CCU. Green light indicates card reader is available for selection at CCU. White light indicates card reader is |

## 2-1. Operator's Controls and Indicators

(fig. 2-1)

CARD JAM indicator Lights (red) when card does not pass through read station within allowable time.
PICK FAIL indicator Lights (red) when card is not (DS8).

CANCEL indicator (DS2). NOT ASSIGNED indicator (DS9).

TEST switch

SINGLE FEED switch-indicator (Z4). indicates (white) momentarily and initiates reading of one card
AUDIBLE RESET switch (Z1). press AUDIBLE RESET switch to remove audible alarm at the CCU.
START switch-indicator (Z7).

| Control or indicator |  |
| :--- | :--- |
| START switch-indicator selected at CCU. Neither in- |  |
| (Z7)-Con. | dicator lights if fault condition |
|  | is present, if card reader is |
|  | stopped, or if card reader is in |
|  | local test operation (initiated |
|  | by LOCAL TEST switch-indi- |
|  | cator). |
| STOP switch-indicator | When momentarily depressed, |
| (Z6). | Stops card feed operations |
|  | initiated by START switch- |
|  | indicator or LOCAL TEST |
|  | switch-indicator. Lights (red) |
|  | when card reader is stopped |
|  | by STOP switch- indicator, |
|  | CANCEL signal, detection |
|  | of a fault condition, an out-of- |
|  | cards condition occurring after |
|  | end of message is acknowl- |
|  | edged by CCU, or power-on |
| Leset. |  |
| LOCAL TEST switch- | When card reader is not |
| indicator (Z5). | assigned and in in the stop |
|  | mode depression of LOCAL |
|  | TEST switch-indicator initiates |
|  | picking and reading of cards in |
|  | local test operation and lights |
| (amber) in this condition. |  |

## 2-2. Types of Operation

a. The card reader can be operated in either the online or local test. mode of operation. Selection of the on-line mode of operation transfers control of the card reader to the CCU. The local test mode is used for test and maintenance.
b. Perform the following sequence of procedures when operating the card reader:
(1) Preliminary starting procedure (para 2-3).
(2) Loading procedure (para 2-4).
(3) Starting procedure (para 2-5).
(4) Operating procedure (para 2-6).
(5) Stopping procedure (para 2-7).

## 2-3. Preliminary Starting Procedure

Press the AC POWER switch-indicator on the control panel. Check to see that the AC POWER and DC POWER indicators are lighted.

## 2-4. Loading Procedure

a. Press the STOP switch-indicator, fan the stack of cards to be read, and square the stack on the card squaring shelf at the right of the control panel.

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Figure 2-1. Control panel controls and indicators.


Figure 2-2. Power supply, front panel.
b. Take about a $1 / 2$-inch thick stack of cards from the top of the deck of cards to be read.
c. Turn the stack face down with row 12 nearest the operator and column 1 to the left.
d. While holding the cards as indicated in step c above, slide the bottom card about $1 / 4$ inch more to tile left; then place the stack into the hopper, sliding the left edge of the bottom card about $1 / 8$ inch into the pneumatic throat. The vacuum at the entrance of the pneumatic throat should pull the bottom card down so that it enters the throat easily.
$e$. Load the rest of the deck of cards to be read face down on top of the loaded cards.
$f$. If the card reader is assigned, press the SINGLE FEED switch-indicator and check to see that the card is fed, read, and stacked properly.

## 2-5. Starting Procedures

a. Press the START switch-indicator on the control panel.
b. Check that the following indicator lamps are not lighted:
(1) STOP switch-indicator.
(2) All fault alarm indicators.

## 2-6. Operating Procedures

a. On-Line Operation. To select on-line operation,
press the START switch-indicator and check that the switch-indicator is lighted green. The cards can then be picked and read in response to step commands from the CCU (switch-indicator lighted (white) during card reading).
b. Local Test Operation. To initiate local test operation, press the STOP switch-indicator, then press the LOCAL TEST switch-indicator and check to be sure the STOP switch-indicator is extinguished.

## 2-7. Stopping Procedure

a. Stop Condition. When in the on-line or local test condition, stop the card reader by pressing the STOP switch-indicator.
b. Power-Down Condition. Press the STOP switch-indicator, then the AC POWER switch-indicator.

## 2-8. Correcting Fault Conditions

When a fault condition occurs, correct it as follows:
a. Check the control panel fault indicators to determine the fault. Note that the fault places the card reader in the STOP condition.
b. Take appropriate action to correct the fault.
c. After the fault is corrected, place the card reader in the on-line condition by pressing the START switchindicator (or in the local test condition by pressing the LOCAL TEST switch-indicator).

## CHAPTER 3

## FUNCTIONING OF CARD READER

## Section I. GENERAL FUNCTIONING OF CARD READER

## 3-1. Card Reader, Block Diagram

fig. 3-1)
All of the card handling and reading functions of the card reader are performed by the card reader mechanism. Within this mechanism, cards are automatically transported by card feed mechanisms from the hopper to the read station, where the punched holes are read, and then to the stacker for storage. Processing of the data read from the cards and control of the card handling operations are performed by electronic circuits in the logic assembly and by manual switches on the control panel. These functions are described in paragraphs 3-2 through 3-8.

## 3-2. Card Feed

Before operating the card reader, standard punched cards (EIA-RS-292) are manually loaded into the hopper which has a 1,000-card capacity. Picking cards from the hopper may be controlled automatically or manually.
a. Remote Operation. Automatic card feed under control of the common control unit (CCU) is accomplished by operation of the START switchindicator on the control panel. This enables card feed control circuits in the logic assembly to operate under CCU control.
(1) The CCU operator must assign the card reader to operate with the CCU by pressing a front panel switch on the CCU. This results in an assigned signal which is routed from the CCU through receive interface circuits to card feed control circuits in the logic assembly of the card reader.
(2) If the card reader is in condition to accept instructions from the CCU, the card feed control circuits generate a ready signal which is routed through transmit interface circuits to the CCU (fig. 3-2). This permits the CCU to select the card reader for a message by sending a select signal and a step/data acknowledge pulse. These signals enable the card feed control circuits to begin card feeding operations.

Note. All signals shown in figure 3-2 are high when active. This format is used in the card reader at the output of the receive interface circuits and at the input of the transmit interface circuits. Conversion by the receive and transmit interface circuits causes most of the actual received and transmitted signals to be inverse (low when active).
(3) The leading edge of the first step/data acknowledge pulse causes the card feed control circuit in the logic assembly to supply a pick command to actuate a pick solenoid in the card feed mechanisms so that a single card is picked from the bottom of the hopper and transported through the read station.
(4) Once a card has been picked, no further control, except offsetting (para 3-6), can be applied to the card until it reaches the stacker. Transport from the hopper through the read station to the stacker is under control of a continuously running $1,725-\mathrm{rpm}$, $1 / 3-\mathrm{hp}$ induction motor in the card feed mechanisms.
(5) As the first card passes through the read station, the 80 columns of data are read and transmitted to the CCU. As each column of data is read, the step/' data acknowledge signal from the CCU drops for an interval of 10 to 100 microseconds $(\mu \mathrm{sec})$. This drop has no effect on the card reader; however, when the step/data acknowledge signal goes back up after the 80th column is read, another card is picked. This process continues until the last card of a message, when the step command does not go back up again after the 80th column is read.
b. Local Operation. When the card reader is not assigned to the CCU, the operator can initiate card feed locally by operation of appropriate card feed switches on the control panel. Continuous card feed (local test operation) can be selected in which a new card is automatically picked as the previous card leaves the read station. Alternately, single-card feed can be selected in which a single card is picked and read each time the single-feed switch-indicator is pressed.

## 3-3. Card Reading

As cards pass through the read station, they are automatically read by a bank of photocells in the read station. There are 12 read photocells positioned to monitor the 12 rows of data on the punched card. When the leading edge of the card passes over the read photocells, all 12 photocells are darkened. Then, as the 80 columns of punched holes pass over the read photocells, an electrical pulse is generated by each photocell as it is uncovered by a punched hole. The speed of motion of the cards past the read photocells is 2.5 milliseconds ( ms ) per column.

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Figure 3-1. Card reader, block diagram.


Figure 3-2. Card reader - CCU interface, timing diagram.

## 3-4. Data Conversion

a. The 12 data lines from the 12 read photocells in the read station represent the information punched in the card column being read. This information is any of 50 characters which can be encoded on the 12 data bits in a column. The 12-bit data format is in the Hollerith code (para 3-8). After storing the 12 data bits in a data register, the bits are converted to an eight-bit ASCII coding format for transmission to the CCU. After conversion in the Hollerith-to-ASCII converter, the data is gated through the transmit interface circuits to the CCU on eight lines if the select signal from the CCU is present. Since this can occur only in CCU operation, no data is transmitted in local test operation (para 3-2).
b. The effect of data conversion is illustrated in figure 3-3 for the characters A through E punched in columns 1 through 5. Note that the character A is represented in the Hollerith code by a hole punched in rows 1 and 12 of the card. This results in pulses from the corresponding read photocells but no pulses from the other photocells. After conversion to ASCII code, pulses of the same pulse width are sent to the CCU on ASCII lines 1,7 , and 8 because that is the ASCII coding for the character A. Similarly, the character B is converted from a Hollerith coding of bits 2 and 12 to ASCII coding of bits 2,7 , and 8.
c. The waveform of a sample Hollerith data output line is shown in figure 3-2. In the sample, it is assumed that pulses are generated for all columns. Since the data signal is derived from the read photocells, it is high when no card is present in the read station as all photocells are lighted at that time. When the leading or trailing edge of the card passes over the read photocells,, the photocells all become darkened, and all data lines go low. This takes approximately 6 ms . As each column of punched holes passes the read photocells, the data lines to be activated go high for a time corresponding to the width of the hole which is approximately 1.5 ms .

## 3-5. Data Strobes

a. To insure that the CCU evaluates the data only in the middle of each data pulse when it is most reliable, the card reader sends a $150-\mu \mathrm{sec}$ data strobe pulse to the CCU near the middle of each data pulse. This function is performed by the data strobe generator which generates 80 data strobes for each punched card synchronized with the 80 columns on the card. The data strobe generator supplies a sample pulse to the data register for each character. The sample pulse enters the 12 data bits of the character in the data register. The data strobe for each character is not generated until after the data is stored, thereby insuring that all data is simultaneously available for transmission to the CCU. There is no delay in the Hollerith-to-ASCII conversion


Figure 3-3. Data conversion, timing diagram.
process so that the data is available for transmission as soon as it is stored in the data register.
b. To aid in synchronizing the generation of data strobes with the holes on the card, the data strobe generator monitors the outputs of the read station photocells, card position signals from other photocells in the read station which monitor the beginning of the card and the end of the card, and timing pulses derived from a timing wheel in the card reader mechanism. The timing pulses enable synchronizing data strobe generation to the motion of the card. Data strobe pulses are gated out to the CCU through the transmit interface circuits only when the select signal is present.

## 3-6. Header Card Offset

A series of cards read in sequence is considered a message. After the last card in a message is read, the CCU drops the select signal for 10 to $100 \mu \mathrm{sec}$. This indicates the next card is the first card of a new message (header card). When this happens, the offset control circuit in the logic assembly actuates an offset solenoid in the card feed mechanisms to offset the

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Figure 3-4. Signaling code chart.
header card from the nearest nonoffset cards by at least 1/4 inch.

## 3-7. Alarm Functions

a. Various operations of the card reader are continuously checked by a group of alarm circuits in logic assembly A1. When an alarm condition occurs, the ready signal to the CCU is interrupted, and an alarm stop or operator's .alarm signal is generated to disable the card feed and is transmitted to the CCU.

Corresponding alarm signals are also fed to indicators on control panel A3 to provide a visual indication of the alarm condition.
b. The following fault conditions call cause all alarm stop:
(1) An invalid character is determined by monitoring the 12 data bit lines from tile read photocells for an invalid combination.
(2) A CCU synchronization (sync) failure is determined by monitoring the end-of-block signal from
the CCU. The end-of-block signal is generated by the CCU immediately following the 80th data strobe of each card (block) and remains active until the first data strobe of the next block. If the end of block signal is not received at the proper time, the CCU is out of sync with the card reader. .Also, at the end of a message, an 81st data strobe must be generated. If not, a CCU sync failure exists.
(3) A light check failure is determined by monitoring the outputs of the 12 read photocells to see if all 12 photocells are lighted when no card is present in the read station.
(4) A dark check failure is determined by monitoring data bits 1 through 8 at the output of the Hollerith-to-AS.CII converter during the time when the leading edge of the card (prior to column 1) is covering the read photocells. The Hollerith character for no holes punched is the space character; therefore, the code contained in ASCII data bits 1 through 8 should be that for a space character. If incorrect, a dark check failure exists.
(5) A card jam condition is determined by monitoring the card position signals from the read station to see if a card remains in the read station longer than 400 ms .
c. The following fault conditions can cause an operator's alarm:
(1) A pick failure is determined by monitoring the card pick command and the card position signals
from the read station to see if a card fails to reach the read station within 115 ms of a pick command.
(2) A hopper empty condition is determined by monitoring the output of a photocell located at the hopper. This photocell is lighted when no cards are in the hopper.
(3) A stacker full condition is determined by the output of a sensing switch at the stacker.
d. In case of an alarm stop or operator's alarm, an audible alarm is sounded in the CCU. The audible alarm for an operator's alarm can be reset by operating a switch on the card reader control panel. Operation of this switch results in transmission of an audible alarm reset signal through the transmit interface circuits to the CCU. In case of an alarm stop, the audible alarm is not reset until the CCU operator operates a cancel switch on the CCU front panel.

## 3-8. Signaling Code

a. The signaling code used by the card reader to transmit data to the CCU is the eight-bit ASCII code shown in figure 3-4. Seven of the ASCII bits contain the data. The eighth is a parity bit which is added or left out as necessary to have odd parity for each character. Figure 3-4 lists the 64 ASCII characters which may be transmitted by the card reader.
b. The data which is punched on the cards being l read is in the 12 -bit FIPS-14 code. This code is shown in figure 3-4 for the 64 characters.

## Section II. MECHANICAL FUNCTIONING OF CARD READER

## 3-9. Reader Mechanism, Block Diagram Card (fig. 3-5)

The card reader mechanism consists of several subassemblies which together perform the card handling functions of the card reader.
a. The cards to be read are placed in the hopper face down. When the picker solenoid is energized by a pick command from the logic assembly, the bottom card is picked lengthwise from the hopper by a vacuum from picker belts, which are pressed against the card by the solenoid. Drive for the picker belts, and for all other rotating mechanisms, is provided by a constantly running motor. The card being picked is held against the picker belts by the suction from a vacuum pump which is driven by the same motor.
b. Reader drive capstans move the card from the picker belts through the read station where 12 read photocells detect the holes punched on the card and generate data signals. The position of the card in the read station is detected by an end of card photocell (placed before the read photocells) and a beginning of
card photocell (placed after the read photocells). All photocells receive light from corresponding illuminating lamps when no card is in the read station. As the card passes through the read station it breaks the lightpath, resulting in a pattern of photocell signals corresponding to the card position and the holes punched on the card. All photocell signals are sent to the logic assembly.
c. When the card leaves the read station it is picked up by the stacker capstan which is driven against the offset idler to send the card into the stacker. If the card is a header card, an offset command energizes the offset solenoid. This adjusts the offset idler to shift the card sideways slightly as it is fed lengthwise into the stacker.
d. To synchronize generation of data strobes (by the logic assembly) with the movement of the cards, a timing gear is mounted on the stacker capstan drive shaft. The evenly spaced teeth on this gear are sensed by a reluctance pickup to generate a sine wave timing signal of eight cycles per column of card travel whose frequency varies with the speed of the mechanism.
e. An indication that the hopper is empty is provided by a photocell located at the hopper. An indication that the stacker is full is provided by a stacker full sensing switch.
$f$. Physically, the picker belts are part of a picker frame assembly, which also includes the hopper empty
photocell and the read station photocells. The read station lamps are part of a light aid idler assembly which also contains the idlers for the reader drive capstans. The card stacking and offsetting functions are performed by the stacker capstan assembly and the offset idler assembly, respectively.


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Figure 3-5. Card reader mechanism, block diagram.

## 3-10. Functioning of Picker Frame Assembly

 (fig. 3-6a. The picker frame assembly consists of four capstan-driven perforated belts, a belt pulley idler, a belt pusher, two reader drive capstans, two vacuum manifolds, and the read photocell support, all of which are mounted on the picker and read head frame. The timing belt, from the stacker capstan shaft turns the input gear on the picker drive shaft which transfers the motion directly to the picker belts and also through timing belts to the reader drive capstans. The four picket belts are turned around the belt pulley idler by a
pulley mounted on the picker drive shaft. The pulley idler is adjustable for varying the belt tension. Two other pulleys, one on each end of the picket. drive shaft, drive timing belts .which transfer motion to the two reader drive capstan pulleys. The two capstans mate with idler rollers which are part of the light station and idler assembly. Depending on the operating speed of the drive motor, the reader drive capstans move a card bat 23.2 to 27.6 inches per second. One complete revolution of the reader drive capstan advances a card exactly 45 columns.


Figure 3-6. Picker frame assembly functional diagram.
b. One end of the belt pusher is attached to the picker and read head frame on a pivot. The free end of the belt pusher includes a vacuum manifold which is pushed up against the perforated belts by the picker solenoid assembly to pick a card from the hopper. The vacuum is applied from the vacuum pump intake through the belt perforations so that the card is gripped and carried by the moving belts. Another vacuum manifold pulls the leading edge of the card flat as it
leaves the belts. This is the part of the picker frame assembly which, together with the light station and idler assembly, forms the pneumatic throat. The pneumatic throat manifold vacuum is formed by air in the vacuum pump exhaust line flowing through a venturi manifold whose throat is connected to the hole in the manifold.
c. The read photocell support includes 14 photocells, 12 of which are positioned to read the 12 rows of
the punched cards. The other two photocells are the end-of-card and the beginning-of-card sensors. The light source for all 14 photocells is supplied by lamps in the light station and idler assembly when the card reader is assembled. The electrical outputs from the phototransistors are brought out to a taper pin block for external connections. One other photocell, located near the downstream end of the picker belt pulley, is used to sense the hopper empty condition. This photocell receives a light source from a lamp on the input card guide and lamp assembly.

## 3-11. Functioning of Light Station and Idler Assembly

## (fig. 3-7)

The light station and idler assembly contains two idler rollers which operate with the reader drive capstan rollers in the picker frame assembly when the card reader is assembled. The light station contains a lamp assembly with 14 lamp filaments that provide light for the 12 read photocells and the end-of-card and beginning-of-card photocells in the picker frame assembly. The throat block is the upper limit of the pneumatic throat when the light station and idler assembly is assembled over the picker frame assembly in the card reader. This pneumatic throat permits only one card at a time to enter the read station.


Figure 3-7. Light station and idler assembly, functional diagram.

## 3-12. Functioning of Stacker Capstan Assembly (fig. 3-8

The stacker capstan assembly receives drive power from a timing belt which is turned by the drive motor. The assembly consists of two pulleys, a 120 -tooth gear, and a capstan roller, all mounted on the same shaft. The 120 -tooth gear is part of the timing generator; the capstan roller is used to drive cards into the stacker. When the card reader is assembled, the capstan roller mates with the idler roller of the offset idler roller assembly. The capstan roller delivers cards to the stacker at approximately 69.6 or 82.8 inches per second, depending on the operating speed of the drive motor (50 or 60 cps ).


Figure 3-8. Stacker capstan assembly, functional diagram.

## 3-13. Functioning of Offset Idler Roller Assembly (fig. 3-9)

In addition to providing an idler roller for the stacker capstan assembly the offset idler roller assembly performs a card-offsetting function. This is used for the header card of a message on command from the logic assembly. The offsetting action is initiated by the offset solenoid which is linked to the bracket supporting the idler roller. When the solenoid energizes, it moves the bracket so that the idler roller is turned slightly off center with respect to the stacker capstan; therefore, as the card is driven lengthwise into the stacker, it is also moved sideways a minimum of $1 / 4$ inch.


Figure 3-9. Offset idler roller assembly, functional diagram.

## 3-14. Functioning of Stacker Assembly <br> (fig. 3-10)

The stacker is basically a flat spring-loaded platform which moves down under the weight of stacked cards. When the number of cards in the stacker reaches capacity, the platform lowers against the load applied by the elevator spring to the preset downward travel limit. Any additional cards loaded into the stacker raise the card deflection plate which then activates the stacker full switch. This produces a signal for the logic assembly which then causes an operator's alarm condition in the card reader.

## 3-15. Timing Generator

(fig. 3-11)
The timing generator performs as a column clock by generating electrical pulses that are mechanically initiated. It consists of a 120 -tooth, 24 -pitch gear and a magnetic pickup assembly. The gear, mounted on the stacker offset capstan shaft, turns at 1,280 rpm or 1,065 rpm , depending on the operating speed of the drive motor. The magnetic pickup is mounted in a fixed position so that the periphery of the timing gear passes the iron core of the pickup.


Figure 3-10. Stacker assembly, functional diagram.
The pickup is adjusted for an airgap of 0.003 inch (nominal) between the core of the pickup and the teeth of the gear.


Figure 3-11. Timing generator, functional diagram.

As a tooth enters the iron core, a pulse is generated first in one direction as the tooth approaches, then in the opposite direction as the tooth leaves the airgap; therefore, the pickup generates a sine wave 120 times for each revolution of the gear. Since the gear makes 3 revolutions for each revolution of the reader drive capstan, 120 times 3 , or 360 sine waves are generated for 45 columns of a card. The result is 8 sine waves per column.

## 3-16. Mechanical Power Distribution System (fig. 3-12)

The mechanical power distribution system supplies the drive for the picker belts, reader drive capstans, stacker capstan, and a vacuum pump. It consists of a drive motor, gears, and timing belts.
a. Drive Motor. The drive motor requires 96 - to 132 -volt, 50 - to $60-\mathrm{cps}$, single-phase ac power and is
rated at $1 / 3$ horsepower. When $60-\mathrm{cps}$ power is supplied, the drive motor speed is $1,725 \mathrm{rpm}$; for $50-\mathrm{cps}$ power, the speed is $1,425 \mathrm{rpm}$. A pulley mounted on one end of the motor armature shaft transfers the driving force to the rest of the system.
b. Power Distribution. The stacker capstan shaft, picker belts capstan, and reader drive capstan shafts rotate continuously when the drive motor is operating. A timing belt transfers power from the motor shaft pulley to the stacker capstan shaft which, in turn, drives the picker drive shaft by a second timing belt. Two other timing belts on the picker drive shaft drive the two transport reader capstan shafts. The vacuum pump is mounted on the rear of the drive motor and is driven directly by the drive motor shaft. The operating speed of each shaft in the system, as well as card travel speeds, is as follows:

| Operating speeds |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input power frequency | Motor | Stacker offset capstan | Picker drive | Transport reader capstans | Reader card travel | Stacker offset capstan travel |
|  |  |  |  |  |  |  |

## 3-17. Deleted



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Figure 3-12. Mechanical power distribution system.

## Section III. ELECTRICAL FUNCTIONING OF CARD READER

## 3-18. Logic Diagrams

a. Most of the data processing and control functions of the card reader are performed by logic circuits on the printed circuit (PC) cards in the logic assembly. The electrical operation of the PC cards are represented in chapter 8 by logic diagrams instead of conventional schematic diagrams. Each logic diagram shows all input and output connections of the card,
including power connections, but does not show the circuit components which make up the individual logic elements.
b. Most of the logic elements in the card reader are mounted in integrated circuit modules, and detailed circuit components are nor applicable. Each integrated circuit logic element is considered to be a single electrical component. For those logic elements

Figure 3-13. Deleted
that are made up of discrete circuit components, the schematic representation and a description of the circuit operation for each type of logic element is given ill paragraphs 3-81 through 3-86

Note. For convenience, all cards in the logic assembly are identified only by their distinguishing reference designations (A1, A2, A3, etc.). It should be understood that these designations are prefixed by A1 (para 1-7).

## 3-19. Logic Signal Notation

a. In general, logic signals in the card reader switch between a. high level of nominally +4.5 volts and a low level of nominally 0 volt. Some signal lines are considered activated when the level is high, and others are considered activated when the level is low. The state indicators (small circles) at the input and outputs of logic elements indicate which lines are activated by a high level (state indicator absent) and which lines are activated by a low level (state indicator present).
b. All significant logic signals are assigned a functional name or designation. To permit the active state of a signal to be indicated by its functional name, the high level is arbitrarily designated true or logic 1 for signal naming purposes, and the low level is arbitrarily designated false or logic 0 . Therefore, the signal is a true-function if it is active on a high level and a notfunction if it is active on a low level. See following mneumonic chart.
c. In the functional descriptions, the terms high and low are used for +4.5 -volt and 0 -volt levels. Pulses
or steps going from 0 volt to +4.5 volts are called positive pulses or steps, and those going from +4.5 volts to 0 volt are called negative pulses or steps.

## 3-20. Logic Diagram Symbol Notation

a. Typical integrated circuit and discrete circuit logic elements are shown in figure 8-10. Inputs and outputs of integrated circuit logic elements are identified by the wire terminal numbers of the integrated circuit modules in which the elements are located.
b. Two tagging lines are used within each logic symbol for identification purposes.
(1) The first tagging line in each logic symbol identifies the logic element type. The various types of integrated circuit and discrete circuit logic elements are described in paragraphs 3-21 through 3-25
(2) The second tagging line in each logic symbol identifies the electrical reference designation of the logic element para $3-21 b$ and $3-24 b$ ). This reference designation is prefixed by the reference designation of the printed circuit card on which it is located.

## 3-21. Integrated Circuit Modules

a. The integrated circuit modules used in the card reader are of several types as described in $b$ through $e$ below; however, they are all of standard construction and wired to the printed circuit cards through 10 terminals ( 1 through 10). Reference designations for the integrated circuit modules are $\mathrm{Z} 1, \mathrm{Z2}, \mathrm{Z} 3$, etc.

## Change 1 3-12

| ABBREVIATIONS AND LOGIC SIGNAL MNEUMONICS AND FUNCTIONAL NAMES |  |  |  |
| :---: | :---: | :---: | :---: |
| AAR | - AUDIBLE ALARM RESET | HL | - HOLLERITH |
| AR | - CHANGE TO NAR | HOL | - HOLLERITH |
| ARC | - AUD RESET SWITCH CLOSED | HOP | - HOPPER PHOTOCELL |
| ARST | - ALARM RESET LOGIC | HPE | - HOPPER EMPTY |
| ARO | - AUD RESET SWITCH OPEN | HPN | - HOPPER PHOTOCELL - NOT |
| AS | - ADVANCE SOLENOID |  |  |
| ASC | - ASCII | INV | - INVALID - CODE |
| ASD' | - ADVANCE SOLENOID DRIVER | INC | - INVALID CHARACTER |
| AST | - ALARM STOP |  |  |
|  |  | LIT | - LIGHT (ALL 12 PHOTOCELLS LIT) |
| BC | - BEGINNING OF CARD | LT | - LOCAL TEST |
| BCN | - BEGINNING OF CARD - NOT | LTC | - LOCAL TEST SWITCH CLOSED |
| BCP | - BEGINNING OF CARD PHOTOCELL | LTO | - LOCAL TEST SWITCH OPEN |
| BLKF | - BLOCK FAILURE |  |  |
|  |  | NAR | - NOT ALARM RESET |
| C5 | - COUNT 5 | NASG | - NOT ASSIGNED |
| CA | - CARD ALARM | NAST | - NOT ALARM STOP |
| CC | - CYCLE COMPLETE | NCAN | - NOT CANCEL |
| C1A9 | - COUNTS 1 OR 9 | NEC | - NOT END OF CARD (FROM PHOTOCELL) |
| CJTP | - CARD JAM TEST POINT | NOA | - NOT OPERATOR ALARM |
| CLK | - CLOCK | NRT | - NOT READ TIME |
| CLTP | - CLOCK TEST POINT | NSEL | - NOT SELECT |
| CYCL | - CYCLE |  |  |
|  |  | OS | - OFFSET |
| DB1 | - DATA BIT 1 (ETC) | OSC | - OFFSET CONTROL |
| DC | - DARK CHECK | OSD | - OFFSET DRIVER |
| DCA | - DISPLAY CARD ALAIRM | OST | - OFFSET TIMER |
| DCAN | - DISPLAY CANCEL |  |  |
| DCE | - DARK CHECK ENABLE | PHCK | - PHOTOCELL CHECK |
| DCF | - DARK CHECK FAILURE A13-10 | PKF | - PICK FAILURE |
| DCJ | - DISPLAY CARD JAM | PRST | - POWER ON RESET |
| DPKF | - DISPLAY PICK FAIL A15-18 | PS | - PICKER SOLENOID |
| DS | - DATA SAMPLE | PRTY | - PARITY |
| DSG | - DISPLAY START-RE |  |  |
| DST | - DATA STPOBE | RASG | - RECEIVE ASSIGNED |
| DSW | - DISPLAY START-WHITE | RCAN | - RECEIVE CANCEL |
| DSYN | - DISPLAY OUT SYN | RDY | - READY |
|  |  | RPA | - RELUCTANCE PICKUP A |
| EC | - END OF CARD-FROM PHOTOCELL | RPB | - RELUCTANCE PICKUP B |
| ECP | - END OF CARD PHOTOCELL | RRST | - REGISTER RESET |
| EOB | - END OF BLOCK | RSB | - RESET BUTTON |
| EOC | - END OF CARD-FROM LOGIC | RST | - RESET |
| EOM | - END OF MESSAGE | RSTO | - RESET SWITCH OPEN |
| GS | - GATED STEP | SC | - START SWTCH CLOSED |

Change 3 3-12.1

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ABBREVIATIONS AND LOGIC SIGNAL MNEUMONICS AND FUNCTIONAL NAMES (cont)

| SDA | - STEP DATA ACK |  |
| :---: | :---: | :---: |
| SEL | - SE ECT |  |
| SEL A | - SELECT A |  |
| SEL B | - SELECT B |  |
| SF | - SINGLE FEED |  |
| SFC | - SINGLE FEED SWITCH CLOSED |  |
| SFO | - SINGLE FEED SWITCH OPEN |  |
| STF | - STACKER FULL |  |
| STFO | - STACKER FULL SWITCH OPEN |  |
| STP | - STOP |  |
| STPO | - STOP SWITCH OPEN |  |
| STR | - STROBE |  |
| XINH | - INHIBIT |  |
| XAM | - AMPERSAND |  |
| XAP | - APOSTROPHE |  |
| XAS | - ASTERISK |  |
| XCA | - COMMA |  |
| XCB | - CLOSING BRACKET |  |
| XCF | - CIRCUMFLEX |  |
| XCN | - COLON |  |
| XCP | - CLOSING PARENTHESIS |  |
| XDR | - DOLLAR SIGN |  |
| XEQ | - EQUAL SIGN |  |
| XEX | - EXCLAMATION POINT |  |
| XGR | - GRAVE ACCENT |  |
| XGT | - GREATER THAN |  |
| XHY | - HYPHEN |  |
| XLT | - LESS THAN |  |
| XNO | - NUMBER SIGN |  |
| XDB | - OPEN BRACKET |  |
| XDP | - OPEN PARENTHESIS |  |
| XPC | - PERCENT |  |
| XPD | - PERIOD |  |
| XPL | - PLUS SIGN |  |
| XQT | - QUOTATION MARKS |  |
| XSC | - SEMICOLON |  |
| XSL | - SLANT |  |
| XSP | - SPACE |  |
| XTL | - TILDE |  |
| XUL | - UNDERLINE |  |
| XVL | - VERTICAL LINE |  |

Change 1 3-12.2
b. Some of the integrated circuit modules contain only one logic element while others contain two. In those cases where two logic elements are contained in one integrated circuit module, the two elements are shown separately on the logic diagrams and are designated A and B (for example: Z 1 A and $\mathrm{Z1B}$ ). The output signal terminal of the A-element in each integrated circuit module is always terminal 2 , and the output signal terminal of the B-element is always terminal 10.
c. Power supply inputs to the individual logic elements are not shown on the logic diagrams since there is no provision for them in logic symbology; however, all integrated circuit modules receive power supply inputs of +4.5 volts at terminal 6 , and 0 volt at terminal 1.
d. Since the integrated circuits are of a standard construction, not all inputs to AND gates and OR gates are used in each application. Unused gating inputs are always wired to one of the used gating inputs; therefore, more than one terminal may be listed at an input on the logic diagram symbol.
e. Most integrated circuit logic elements can function in more than one way. Every AND gate for high inputs is an OR gate for low inputs and every OR gate for low inputs is an AND gate for high inputs. A noninverting OR gate becomes a simple buffer if the inputs are wired together, and an inverting OR gate becomes an inverter if the inputs are wired together. The logic operation of each integrated circuit module type is described in paragraph 3-22.

## 3-22. Operation of Individual Integrated Circuit Modules

The operation of the individual integrated circuit modules used in the card reader is described in a through $h$ below. Logic symbols are given for each type of module, using typical tagging lines.
a. Type A-1 Module. Two type A-1 gates are located on each type A-1 module fig. 3-14) These may be noninverting AND gates for high inputs (case A) or noninverting OR gates for low inputs (case B). Open circuit inputs are equivalent to high levels.


Figure 3-14. Type A-1 module, logic symbol.
b. Type E-1 Module. Two type E-1 gates are located on each type E-1 module (fig. 3-15) These may be noninverting OR gates for high inputs (case A) or noninverting AND gates for low inputs. The type E-1 gate outputs are used only as expander inputs for $\mathrm{N}-3$ or O-3 modules ( $e$ and $g$ below). Open circuit inputs to type E-1 gates are equivalent to low levels.
c. Type N-1 Module. Two type N-1 gates are located on each type $\mathrm{N}-1$ module fig. 3-16). These may be inverting OR gates for high inputs (case A) or inverting AND gates for low inputs (case B). The type $\mathrm{N}-1$ gates may also act as simple inverters (case C). This is accomplished by tying all input terminals together. Open circuit inputs are equivalent to low levels.
d. Type $\mathrm{N}-2$ Module. A single type $\mathrm{N}-2$ module (fig. 3-17) is used in the card reader on PC card A13. This module contains a single inverting AND gate for low inputs.
e. Type $\mathrm{N}-3$ Module. Two type $\mathrm{N}-3$ gates are located on each type $\mathrm{N}-3$ module (fig. 3-18). These may be inverting OR gates for high inputs (case A) or inverting AND gates for low inputs (case B). The type $\mathrm{N}-3$ gates are used with an expander input supplied by type E-1 OR gates for case A and by type E-1 AND gates for case B. Open circuit inputs are equivalent to low levels.
f. Type O-1 Module. Two type O-1 gates are located on each type $\mathrm{O}-1$ module fig. 3-19). These may be noninverting OR gates for high inputs (case A) or noninverting AND gates for low inputs (case B). The type O-1 gates may also act as simple buffers (case C). This is accomplished by tying all input terminals together. Open circuit inputs are equivalent to low levels.
g. Type O-3 Module. Two type O-3 gates are located on each type O-3 module fig. 3-20). These may be noninverting OR gates for high inputs (case A) or noninverting AND gates for low inputs (case B). The type O-3 gates are used with an expander input supplied by type $\mathrm{E}-1$ OR gates for case $A$


Figure 3-15. Type E-1 module, logic symbols.


Figure 3-16. Type $\mathrm{N}-1$ module, logic symbols.
and by type E-1 AND gates for case B. Open circuit inputs are equivalent to low levels.
h. Type FF-1 Module. One type FF-1 flip-flop is located on each type FF-1 module (fig. 3-21).
(1) In the case A configuration, the flip-flop can be set by either a high level at the S-input or a high level at the J-input which is clocked by a negative step at the CL-input. The flip-flop can be cleared by either a high level at the C-input or a high level at the K-input which is clocked by a negative step at the CL-input.
(2) In the case B configuration, terminals 4, 5, and 7 are tied together to form a T-input. When the Sand C-inputs are low, the flip-flop is toggled between the set and clear states by negative steps at the T-input; otherwise, the flip-flop is set by a high level at the Sinput and cleared by a high level at the C-input.
(3) Open circuits at the J-, K-, CL-, or Tinputs are equivalent to high levels. Open circuits at the S- or C-inputs cause intermittent erroneous changes of state.


Figure 3-17. Type $\mathrm{N}-2$ module, logic symbol.


Figure 3-18. Type $\mathrm{N}-3$ module, logic symbols.
(4) Unused J- and K-inputs are wired to terminal 1 ( 0 volt). To permanently enable J-, K-, or CLinputs, these inputs are wired to terminal 6 ( +4.5 volts).

## 3-23. Integrated Circuit Latch

a. A special combination of $\mathrm{N}-1$ OR gates called a latch (fig. 3-22) is used extensively in the card reader logic circuits. The latch functions as a flip. flop to register the occurrence of momentary signals. The two OR gates which make up the latch are called the set and clear sides of the latch. The 1 output of the latch goes high when the latch is set, and the 0 output goes high when the latch is cleared.
b. To set the latch, both inputs to the clear side must be low, and a high level must occur at either of the two inputs to the set side. The resulting low output of the set side then causes the clear side to produce a high level on the 1 line. This high level maintains an input to the set side so that even if the external input goes low, the latch remains set.
c. To clear the latch, both inputs to the set side must be low and a high level must be applied to either clear side inputs. This causes the 1 output to go low and the 0 output to go high; therefore, the clear condition is reinforced and remains, even after the high level to the clear side goes low again.


Figure 3-19. Type 0-1 module, logic symbols.

## 3-23.1 Microcircuit Logic Elements

a. Lamp driver circuits used in the card reader consists of thick film circuit components encapsulated within a square plastic case. These circuits are type SM-63 microcircuits, and are wired to the printed circuit cards through 10 terminals ( 1 through 10). Reference designations of the microcircuit modules are $\mathrm{Z} 1, \mathrm{Z} 2, \mathrm{Z} 3$, etc. Each microcircuit module contains three separate circuits. These circuits are shown separately on the logic diagrams and are designated as $\mathrm{A}, \mathrm{B}$ and C . (For example: Z1A, Z1B and Z1C.) The output terminals from the A circuit is always terminal 1 ; for the $B$ circuit terminal 3 ; and for the C circuit, terminal 5
(see fig. 3-22.1.
b. Power supply inputs to the individual microcircuit modules is not shown on the logic diagrams since there is no provision for them in logic symbology. However, all lamp driver SM3-63 microcircuit modules receive power supply inputs so +12 volts at terminal 7 , 12 volts at terminal 8 , and ground at terminal 10.
c. The lamp driver provides a current return path for indicator lamps. One side of the indicator lamp is connected to +15 volts ac and the other side is connected to the output terminal of the lamp driver. With no input (0 level) to the lamp driver, an internal resistor provides a high resistance path to ground to maintain a warming current on the lamp even though it is not lighted. When a high logic level is applied to the
input to the lamp driver, the output terminal becomes a low resistance high current path to ground for the lamp, and the lamp lights.
d. Terminal 9 of all lamp driver modules are wired to LAMP TEST switch A3Z3 which applies +12 volts dc to the lamp driver when actuated. This voltage switches he lamp driver on to light the lamp.


Figure 3-22.1. Microcircuit lamp driver logic symbol.

## 3-23.2 Transmitter and Receiver Microcircuit Logic Elements

Some models of the Card Readers use thick film microcircuits as interface transmitters and receivers on PC cards A4 and A5. The microcircuits are constructed similar to the microcircuit lamp drivers (para 3-23.1) but are wired to' the printed circuit board through 14 terminals ( 1 through 14). Four types of transmitter and receiver microcircuits are supplied. Operation of each type is described in the following paragraphs.
a. Type T00023 Polar Transmitter. Polar transmitters convert a 0 volt logic level to a-6 volt output, and a +4.5 volt input to a +6 volt output. Provisions are made to AND up to three input signals to the polar transmitter. When this option is used, all inputs must be high before +6 volts is transmitted. When one or more inputs are low, -6 volts is maintained at the output. Five slightly different variations of polar transmitter microcircuit modules exist, because of different output rise and fall time characteristics and number of inputs that may be ANDed together. Inputs are ANDed by applying the signals to terminals of the microcircuit module designated as diode inputs. If the output signal is applied to the direct input terminal, the output signal switches between -6 and +6 volts as the input signal varies between 0 and +4.5 volts, as described previously. Each type of polar transmitter is identified by the basic type number (T00023) and a dash number. Power supply inputs, and input and output terminals for each dash number polar transmitter is shown below. A dash in the chart indicates no connection for that function. Terminals not listed are not used.

|  | Terminal Number T00023 |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Function -001 | -002 | -003 | -004 | -005 |
| Direct input............. 14 | 14 | 14 | 14 | 14 |
| Diode input 1............. 2 | 2 | -- | 2 |  |
| Diode input 2............ 3 | 3 | -- | 3 | -- |
| Diode input 3........... 12 | -- | -- |  |  |
| Output..................... 8 | 8 | 8 | 8 | 8 |
| +12 volt dc supply .... 13 | 13 | 13 | 13 | 13 |
| --12 volt dc supply...... 1 | 1 | 1 | 1 | 1 |
| Ground.................... 7 | 7 | 7 | 7 | 7 |

b. Type T00024 Polar Receiver. Polar receivers convert a +6 volt input to +4.5 volts and a -6 volt input to 0 volts. Provision is also made to allow the receiver output to be clamped to the 0 volt output level by applying a high level on the inhibit output. Two variations of polar receiver microcircuit module are supplied. One (T00024001) contains two separate but identical circuits inside the module while the other (T00024-002) contains a single receiver circuit. Power supply and input and output connections for the polar receivers are shown below. A dash in the chart
indicates no connection for that function. Terminals not listed are not connected.

| Function | Terminal number T00024 |  |
| :---: | :---: | :---: |
|  | -001 | -002 |
| Input No. 1. | .. 1 | 1 |
| Output No. 1 | . 11 | 11 |
| Inhibit No. 1. | ... 13 | 13 |
| Input No. 2 |  | -- |
| Output No. 2 | . 9 | -- |
| Inhibit No. 2. | . 2 | -- |
| +12 volt dc supply . | ... 12 | 12 |
| -12 volt dc supply.. | ..... 6 | 6 |
| +4.5 volt de supply ... | ....... 10 | 10 |
| Ground. | . 4 | 4 |

c. Type T00121 Neutral Receiver. Neutral Receivers convert a 0 volt input from the CCU to +4.5 volts and an open circuit input to 0 volts. In addition, some variations of the microcircuit neutral receivers have provisions for maintaining the output at 0 volts by application of a separate inhibit signal. Four variations of neutral receiver microcircuits are supplied, with the differences being in the number of separate circuits contained in each module and inhibit levels used. Microcircuits T00121-001 and -002 contain three similar, but separate, receiver circuits, while T00121003 and 004 modules contain only two. The T00121-002 and 004 modules also provide connections for inhibit signals. Inhibit A requires a high level to clamp the output to 0 volts, and inhibit B requires a low level ( 0 volt) signal to maintain the 0 volt output. The chart below shows input, output, and power supply connections for the neutral receivers. A dash in the chart indicates no connection for that function. Terminals not listed are not connected.

| Function | Terminal Number T00121 |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | -001 | -002 | -003 | -004 |
| Circuit 1: |  |  |  |  |
| Direct input- .... | ... 14 | 14 | 14 | 14 |
| Diode input...... | ... 12 | -- | -- | -- |
| Inhibit $\mathrm{A}^{\text {a }}$. ...... |  | -- | -- | 3 |
| Inhibit ${ }^{\text {b }}$ |  | 3 | -- | -- |
| Output............ | .. 8 | 8 | 8 | 8 |
| Circuit 2: |  |  |  |  |
| Direct input...... | ... 13 | 13 | 13 | 13 |
| Diode input...... |  | -- | -- | -- |
| Inhibit B ${ }^{\text {......... }}$ | .. -- | 4 | -- | -- |
| Output.......... | . 10 | 10 | 10 | 10 |

a. Requires high level to inhibit
b. Requires low level to inhibit

|  | Terminal Number T00121 |  |  |  |
| :--- | ---: | ---: | ---: | ---: |
| Function | -001 | -002 | -003 | -004 |
| Circuit 3: |  |  |  |  |
| Diode input.. ............ 9 | 9 | - | -- |  |
| Output.................. 6 | 6 | -- | -- |  |
| +12 volt dc supply...... .11 | 11 | 11 | 11 |  |
| -12 volt dc supply....... | 1 | 1 | 1 |  |
| +4.5 volt dc supply ....... 7 | 7 | 7 | 7 |  |
| Ground................... 5 | 5 | 5 | 5 |  |

d. Type T00122 Neutral Transmitter. Neutral transmitters convert +4.5 volt logic levels to 0 volts for transmission and low level inputs to an open circuit. Four variations of neutral transmitter are supplied, with each having two or three similar, but separate, circuits and diode inputs which may be connected to provide an AND function for input signals. The following chart lists the input, output, and power supply connections for the neutral transmitters. A dash in the chart indicates no connection for that function. Terminals not listed are not connected.

|  | Terminal Number T00122 |  |  |
| :---: | :---: | :---: | :---: |
| Function -001 | -002 | -003 | -004 |
| Circuit 1: |  |  |  |
| Direct input ........... 13 | 13 | 13 | 13 |
| Diode input ............. 2 | 2 | -- | 2 |
| Diode input ............. 3 | 3 | -- | 3 |
| Output................... 1 | 1 | 1 | 1 |
| Circuit 2: |  |  |  |
| Diode input ........... 10 | -- | -- | -- |
| Diode input ........... 11 | -- | -- | -- |
| Output................... 5 | -- | -- | -- |
| Circuit 3: |  |  |  |
| Direct input ............. 8 | 8 | 8 | 8 |
| Diode input ............. 9 | 9 | -- | -- |
| Diode input ............. 6 | 6 | -- | -- |
| Output................... 7 | 7 | 7 | 7 |
| +12 volt dc supply ....... 12 | 12 | 12 | 12 |
| -12 volt dc supply ........ 14 | 14 | 14 | 14 |
| Ground........................ 4 | 4 | 4 | 4 |

e. Transmitter and receiver microcircuit modules are connected through 14 terminals. Figure 5-1.1 shows the location of these terminals.

Change 4 3-14.3/(3-14.4 blank)


Figure 3-20. Type 0-3 module, logic symbols.

## 3-24. Discrete Circuit Logic Elements

a. There are several types of discrete circuit logic elements as described in paragraph 3-25. Each discrete circuit logic element consists of a combination of standard circuit components such as resistors, diodes, etc.; therefore, wire terminal numbers for inputs and outputs are not assigned as they are for integrated circuit logic elements.
b. Reference designations for discrete circuit logic elements are (A), (B), (C), etc., prefixed by the reference designation of the printed circuit card on which they are located.

## 3-25. Operation of Discrete Circuit Logic Elements

The logic operation of each discrete circuit logic element type is described below. Logic symbols for each type are given, using typical tagging lines. The logic elements are grouped by the card on which they are located. Schematic diagrams and detailed circuit operation of each type of discrete circuit logic element are given in paragraphs 3-81 through 3-86.
a. PC Card A4. The following discrete circuit logic elements are located on PC card A4 (fig. 3-23).


CASEA

case:
TM4440-220-15-24

Figure 3-21. Type FF-1 module, logic symbol.


Figure 3-22. Latch logic symbol.
(1) Type XMTR-1A. The type XMTR-1A interface transmitter converts a low level input from the card reader to an open circuit for the CCU and a high level input to $\mathbf{O} \mathbf{v}$ for the CCU.
(2) Type XMTR-1B. The type XMTR-1B interface transmitter transmits 0 volt to the CCU when both inputs are high. When one or both inputs go low, an open circuit is transmitted to the C,U.
(3) Type RCVR-1A and RCVR-1B interface receiver converts a 0 -volt input from the CCU to +4.5 volts and an open circuit input from the CCU to 0 volt.
(4) The Type RCVR-1C interface receiver converts a +6.2 volt input from the CCU to +4.5 volts and an open circuit input to 0 volt.
b. PC Card A5. PC card A5 contains a single type of discrete circuit logic element. This is the type XMTR2 interface transmitter (fig. 3-24) which transmits +6.2 volts to the CCU when both inputs are high. When one or both inputs go low, -6.2 volts is transmitted to the CCU.


TM7440-215-13-23
Figure 3-23. PC card A4 discrete circuit logic element symbols.


## INTERFACE TRANSMITTERS

TM7440-215-15-24
Figure 3-24. PC card A5 discrete circuit logic element symbols.
c. PC Card A16. PC, card A6 contains a single type of discrete circuit logic element. This is the type PHOTO AMPL photocell amplifier (fig. 3-25 which converts a dark photocell output (low current) to a high level and a light photocell output (high current) to a low level.

## 3-26. Ac Circuits <br> (fig. 8-5

The ac input circuit receives the external ac power and distributes the power to the various circuits of the card reader. The 120 -volt, single-phase input power is routed through power filters FL1 through FL4 of filter assembly FL1 to power supply terminal board TB1. The filters eliminate high frequency noise from the ac input. The ac power is switched through power supply PS1 to cabinet blower B1 and to the card reader mechanism. Switching control to PS1 is provided by AC POWER switch indicator Z2 on the control panel. Power supply PS1 produces a 24 -volt dc output which, when returned through the closed contacts of AC POWER switch indicator Z2 and sequence module A12 in the power supply PS1, turns on ac power to the card reader mechanism drive motor and cabinet blowers. When power is turned on, the 24 -volt dc output turns on the indicator in AC POWER switch-indicator Z2. The power supply also provides 15 -volt ac power for illuminating the various indicator lamps on the control panel of the card reader.

## 3-27. Dc Circuits

(fig. 8-6
Tile dc voltages required by the card reader are generated in power supply PS1. The following regulated voltages are supplied: +12 volts de, -12 volts de,+4.75 volts de, and -48 volts de. These voltages are automatically turned on in a specific sequence, as


Figure 3-25. PC card A6 discrete circuit logic element symbol.
controlled by a sequence module in the power supply, to supply bias voltages to circuit elements in such as manner that no damage is done to these elements: , Also, in case of a failure in any one of the dc supplies, or when the equipment is turned off, the power supplies are turned off in a predetermined sequence. Turn-on and turn-off of the dc power supplies controlled by the AC PONWER pushbutton Z2. DC POWER indicator DS1 on the control panel indicates when the dc power supplies have been turned on. The reason for using the same switch to turn on ac and dc power is that the sequence of power turn on requires ac power to be supplied to the drive motor and blowers before turning on the dc power supplies.

## 3-28. Power Supply PS1, Block Diagram

The power supply consists of four similar regulator circuits, each containing overvoltage and current limiting circuits, which provide regulated $+4.75 \mathrm{vdc},+12 \mathrm{vdc}$, $12 \mathrm{vdc}, 48 \mathrm{vdc}$ regulated power for the card reader. Also included in the power supply is a sequencing circuit which turns on and off the regulators and the ac power to the drive motor and fans in a predetermined manner when the card reader is started or stopped. The sequencing circuit also turns off the regulators and the drive motor and fans is there is a failure in any portion of the power supplies. Fuses mounted on the front panel of the power supplies, protect each regulator assembly, the ac power lines to the drive motor and fans, and the main ac power transformer in the power supply. The AC POWER switch-indicator on the control panel of the card reader is used to turn the power supply on and off. The sequencing circuit lights the lamps in the switch-indicator when the power supply is on.

## 3-29. Rectifiers and Voltage Regulators

## (fig. 3-26)

a. The power supply receives 120 volt, 50 or $60-\mathrm{hz}$ ac power, which is applied to the primary of the main power transformer. Ac voltages from secondary windings are applied to five full-wave rectifier and filter networks, four of which supply input dc voltages to the four regulator circuits; and the fifth rectifier supplies the unregulated 24 -volt do power required by the sequence module.
b. The four regulating circuits operate in a similar manner; therefore, only the +4.75 vdc regulate is illustrated in figure 3-26 and is described.
(1) A nominal +10 vdc is supplied from the rectifier and filter to a series regulator circuit in the +4.75 -volt regulator. The series regulator, under the control of the regulator control circuit, acts as a variable resistance load which reduces the unregulated 10 volts dc to an accurately regulated +4.75 volts dc.

Variations in the output voltage from this value are sensed by the voltage sensor network, which applies a corresponding control voltage to the regulator control circuit. This circuit, in turn, controls the series regulator in a manner which changes the voltage drop across this circuit by the proper amount to maintain the output voltage at +4.75 volts dc.
(2) As a safety feature, an overvoltage sensor circuit and an over current sensor circuit are included in the regulator circuits. If the output voltage should momentarily rise above 115 percent of the rated output, this is sensed by the sensor. A control voltage is then applied to the regulator control circuit to cause the series regulator to produce a sharp drop in the output voltage. This action should return the regulator circuit to the proper output voltage. If the overvoltage condition is caused by a failure in the regulator circuit, instead of a transient condition, it cannot be corrected by the overvoltage circuit. In this case, the excessive voltage causes the fuse at the input of the series regulator circuit to blow, protecting the regulator from further damage.
(3) If the output current rises above 120 percent of rated value, this is sensed by the over current sensor, which provides a control voltage to the regulator control circuit to cause the series regulator to produce a sharp output voltage drop which practically turns off the series regulator. A corresponding severe current drop is produced. This action produces current limiting during load faults in which the short circuit currents are less than the rated currents, effectively minimizing power dissipation at these times.

## 3-30. Power Turn-On, and Turn-Off Sequencing Control

> (fig. 3-27)
a. To minimize the initial power drain at turn-on of the card reader by AC POWER switch-indicator, and to protect the electronic circuits in the card reader from damage cause by the improper sequence of application of bias and control voltages when power is initially turned on, the various dc voltages required by these circuits are supplied by the power supply in a specific predetermined sequence. Also, whenever the card reader is turned off by the AC POWER switch-indicator, the power supplies are automatically shut down the opposite sequence to turn-on, with certain specific delays between individual power turn-offs being included. In addition, if there is a failure in any of the circuits of the power supply, the complete power supply is automatically shut down in a specific sequence, again protecting the card reader circuits from damage due to improper operating voltages. The sequencing circuit also controls the turn-on and turn-off of the ac power to the drive motor and the fans, assuring that this power is
supplied before the various dc voltages are supplied and turning off this power when the card reader is shut down or when there is a failure in the power supply. The 15volt ac lamp power for the AC POWER switch-indicator and the other indicators of the card reader control panel are also controlled by the sequencing circuits. When power is turned off, all lamps will be dark.
b. The automatic power sequencing circuits are all contained on sequence module A12, and consist basically of two types of voltage level sensors. One type senses whether each of the regulated dc output voltages is within 90 percent of rated output level and the other type senses when the output level of certain of the power supplies falls below 1.8 volt or 10 percent of rated value, whichever is higher. The 90 percent of rated value represents the minimum output voltage level at which a regulator is considered on and operating normally. During the turn-on sequence, these sensors determine when a particular regulator is on and providing the proper output voltage amplitude, and then provide the control to turn on the next, regulator in the power turn-on sequence. The 90 percent sensors are also used to sense if there is a less than normal output from a regulator, indicating a failure in this regulator. If this occurs, the particular sensor involved initiates and automatic turn-off procedure which turns off all the regulators in the proper sequence.
c. The turn-off procedure for each regulator is a two-stage action. First the regulator output-voltage is reduced to a value of approximately 10 percent of rated value (or 1.8 volt, as applicable). The regulator is then considered to be off. At a later stage of the turn-off sequence, a second control action is applied from the sequence module to the regulator to completely turn off the output. voltage.
$d$. The operating voltage for the sequence module is supplied by the 24 --volt rectifier-filter. This voltage is converted to a regulated 15.0 volts de, which is used as the bias and collector voltages for the transistors of the sequence module. A 90 percent fault sensor monitors the output of this regulator as part of the overall power failure monitoring control. The sequence module operates in the following manger.
(1) When the AC POWER switch-indicator is depressed to start operation of the card reader, it momentarily applies the 24 volts de from the 24 -volt dc rectifier-filter network to a self-latching relay in the sequence module. This energizes the relay, which holds itself energized after the AC POWER switch indicator is released. The latching relay applies the 24 volts dc to a relay driver in the sequence module, which then energizes the ac power relay. This applies the auxiliary ac power to the drive motor, the fans, and to all control panel indicator lamps. The AC


Figure 3-26. Rectifiers and voltage regulators, block diagram.


Figure 3-27. Power sequencing circuit, block diagram.
3-18.1 (3-18.2)

POWER switch-indicator lights to indicate that the ac power is now on. In addition, the 24 volts dc is applied to the 15.0 -volt de regulator in the sequence module which produces a regulated 15.0 -volt dc output which is required to operate the other circuits of the sequence module. This action is the start of the automatic turn-on for the four regulators. The regulators are turned on in the following sequence: -12 volt dc, +4.75 volt dc, +12 volt dc, and --48 volt dc.
(2) When the output of the 15.0 -volt regulator reaches 90 percent of rated value ( 12 volts de), the + 15.0 -volt 90 percent sensor applies a bias voltage to the series regulator of the -12-volt regulator circuit. Until this bias is applied, the regulator circuit is disabled and produces no output. A sample of the outputs of all the regulators are applied to individual 90 percent sensors on the sequence module. Thus, when the output of the --12-volt regulator builds up to at least 90 percent of rated value ( -10 volts de), the --12-volt 90 percent sensor applies a turn-on bias to the +4.75 -volt regulator, to turn on this regulator. This action continues, with the applicable 90 percent sensors applying a turn-on bias to the corresponding voltage regulator.
(3) The turn-off sequence is started by again pressing in the AC POWER switch-indicator. This action applies the 24 -volt dc power to a pulse generator which produces a pulse which is applied to the overvoltage sensor circuit of the -48-volt regulator to cause this circuit to sharply reduce the output voltage of the -48 -volt regulator. When the output voltage drops to 10 percent of rated value, or less, the regulator is considered to be off. A -48-volt 10 percent voltage sensor senses that the voltage has dropped to the off amplitude and it applies a gate voltage to the overvoltage sensor circuit in the +12 -volt regulator to turn off this regulator. As the output voltage of the $+12-$ volt regulator now drops below 90 percent of rated value, this is sensed by the +12 -volt 90 percent sensor. The sensor now removes the series regulator bias from the -48-volt regulator circuit (previously turned off to less than 10 percent of rated output),-completely turning off the 48 -volt regulator. As the output of the +12 -volt regulator continues falling to 10 percent of rated value, the +12 -volt 10 percent level sensor senses this condition and applies a gate voltage to the overvoltage sensor circuit of the +4.75 -volt regulator. This action turns off the +4.75 -volt regulator. The action continues in a manner similar to that previously described in the following sequence. The +4.75 -volt 90 percent sensor turns off the +12 -volt regulator completely. Then the + 4.75 -volt 10 percent sensor applies a voltage to the relay driver clamp, which deenergizes the ac power relay removing the ac power from the drive motor and fans At the same time, the voltage from the +4.75 -volt 10 percent sensor is applied to a $300-\mathrm{ms}$ timer.

Approximately $300-\mathrm{ms}$ later, the timer circuit operates a pulse generator which generates a pulse to turn off the 12 -volt regulator. The 12 -volt 90 percent sensor then completely turns off the +4.75 -volt regulator. The pulse produced by the pulse generator is also applied to the turn-off control for the latching relay. The turn-off control then deenergizes the relay, interrupting the 24volt dc power applied to the +15.0 -volt do regulator. This completes the sequenced power turn-off procedure.
e. If there is a failure on any of the power supplies, the complete power supply is automatically shut down in a predetermined sequence which is somewhat different from the normal shutdown sequence. A regulator is assumed to have failed if its output voltage drops to 90 percent., or less, of rated output. If the -48 -volt, $+12-$ volt, or +4.75 -volt supply fails, all of these three supplies are turned off simultaneously, and then, after the same $300-\mathrm{ms}$ time delay required for the normal turn-off procedure, the -12 -volt supply is turned off, as is the ac power and the regulator +15.0 -volt supply. If the $12-$ volt supply has failed, the other supplies are turned off simultaneously and if the 15 -volt regulator in the sequence module fails, this initiates turn-off of the 12volt supply to produce complete power shutdown. A failure in a supply is sensed by the 90 percent sensor associated with that supply. The sensor then operates a silicon control rectifier (SCR) driver to initiate turn-off by firing the associated SCR in the applicable regulator. A single SCR driver is controlled by any one of the 90 percent sensors for the four regulators, and this SCR turn off the -48 -volt, +4.75 -volt, and +12 -volt regulators simultaneously. The 12 -volt regulator is then turned off in the normal manner.
$f$. The SCR driver used for turn-off if a failure is detected must be prevented from operating during power turn-on. This is accomplished by the driver clamp timer and driver clamp circuit, which inhibits the SCR driver for a period of 1.8 second after the start of power turn-on. The same circuit inhibits the operation of the 10 percent sensors during turn-on, since these sensors would also interfere with the turn on sequence. During the normal turn-off sequence, the SCR driver must again be inhibited; otherwise it would interfere with the normal turn-off sequence. This is accomplished by the $80-\mathrm{ms}$ timer.

## 3-31. Detailed Circuit Description of Rectifiers and Voltage Regulators

(fig. 8-7)
a. Input Rectifier Circuits. The power supply receives 115 -volt, 50 or $60-\mathrm{hz}$ ac power at terminals 1 and 2 of terminal board TB1. A 10-ampere fuse A10XF5 is included in the line from the terminal
board to the primary of transformer A9T1. The secondary of this transformer provides ac voltages to four full-wave rectifiers. The full-wave rectifiers are as follows: diodes A4CR4 and A4CR3, with filter capacitor A9C6 provide a nominal 68 volt de input to the -48 -volt dc regulator circuit; diodes A5CR3 and A5CR4 with filter capacitor A9C5 provide a nominal -20-volt dc input to the -12 -volt dc regulator circuit; diodes A5CR1 and A5CR2 and filter capacitor A9C4 provide a nominal $+20-$ volt de input to the +12 -volt do regulator circuit. Diodes A4CR1 and A4CR2 with filter capacitors A9C2 and A9C3 provide a nominal +10 volts dc for the +4.75 volt dc regulator.
(1) A pair of ac outputs are picked off taps 9 and 7 and 5 and 7 of the secondary of transformer A9T1 to provide $15-0-15$-volt ac power for the indicator lamps of the card reader. Fuses A10XF9 and A10X10 are included in each line to protect the transformer from an overload. The application of the 15 -volt ac lamp illumination power is controlled by relay A9K1, as is the ac power to the drive motor and fan. The relay is energized by the sequence module as part of the power turn-on procedure.
(2) A second output winding, taps 12 and 13 on transformer A9T1, provides a nominal 23 -volt ac input to full-wave bridge rectifier A15CR1, A15CR2, A15CR3, A15CR4, and filter capacitor A9C1 provides a nominal 24 -volt do input to the sequence module (para 3-32.
b. +4.5 -Volt Dc Regulator Circuit.
(1) Voltage regulation. The unregulated 10volt dc output of rectifier A4CR1 and A4CR2 is applied through fuse A10FX1 to the series regulator consisting of transistors A4Q1 and A4Q2 connected in parallel. The transistors act as a variable resistance in series with the 10 volts dc to drop this voltage to +4.75 volts at the output of the regulator (junction of A4R1 and A4R2). The regulator control circuit senses variations in the output voltage from +4.75 volts and adjusts the voltage drop across the series regulator transistors to compensate for these variations, thus maintaining a $+4.75-$ volt dc output.
(a) The 10 volts dc is applied to the collectors of transistors A4Q1 and A4Q2 connected in parallel. The voltage drop across the transistors is controlled by the base voltage applied to the transistors, which is supplied by the regulator control circuit. The outputs of the two transistors are taken from their emitters and coupled through emitter resistors A4R1 and A4R2, respectively to a junction point and to the regulator output terminal, pin 2 of TB2. The resistors provide emitter degeneration to assure satisfactory current sharing between the two series regulator transistors.
(b) Zener reference diode AICR6 provides a regulated voltage to a voltage divider consisting of A1R23, A1R24, and A1R25, which provides a fixed bias to the base of A1Q5, part of differential amplifier A1Q5 and A1Q6. A sample of the output voltage of the regulator is applied to the base of A1Q6. The wiper arm of potentiometer A1R24 is set so that, during the stable condition of the regulator, the proper, voltage is picked off this voltage divider to operate the regulator circuit to provide a +4.75 -volt dc output. Should the output voltage vary from this value, the voltage at the base of A1Q6 increases or decreases proportionately, producing a corresponding variation in the output voltage of A1Q6. Since the base of A1Q5 is held at a constant voltage by Zener regulator diode A1CR6, the common emitter of A1Q5 and A1Q6 is held at a voltage which only varies with variations in transistor characteristics or variations in bias. However, since transistors AiQ6 and A1Q5 are of the same type, temperature variations, bias voltage variations, aging, and other variations of this type have the same effect on both transistors and there is no net change in the base-to-emitter voltage at A1Q6. Only a change in the base voltage at A1Q6 produces a net change in the collector voltage at A1Q6. The voltage at the collector of A1Q6 is applied to the base of A1Q1. If there has been an increase in the regulator output voltage above +4.75 volts, the voltage applied to A1Q1 decreases, decreasing the voltage at the base of emitter follower A4Q3, which reduces the voltage at the parallel bases of series regulators A4Q1 and A1Q2. The voltage drop across these transistors increases, reducing the output voltage back down to +4.75 volts dc. A similar analysis applies if the output voltage has fallen below +4.75 volts dc.
(c) The emitter follower stage A4Q3 is used as a current amplifier to provide adequate current amplification for the series regulator.
(2) Current limiting.
(a) The sum of the currents at the emitters of series regulators A4Q1 and A1Q2 is the output current of the voltage regulator. Parallelconnected resistors A1R4 through AIR9 comprise a summing network which samples this current and provides a proportional voltage at the base of A1Q4. By biasing diode AICR4 in a forward direction, the net basemitter threshold voltage for A1Q4 is set to cut off A1Q4 during normal operation. The use of diode A1CR4 to establish base bias provides temperature stabilization and permits operation at low signal levels.
(b) If the load current on the series regulator increases to 120 percent of rated value, the voltage drop across current-sensing resistors A1R4 through

A1R9 increases sufficiently to turn on A1Q4. This causes a sharp voltage drop at the collector of A1Q4, which is connected to the base of A1Q1, producing a corresponding -voltage drop at the base of A1Q1 whichseverely reduces the conduction of series regulators A4Q2 and A4Q1. This action causes a sharp decrease in output voltage, further forward-biasing A1Q4, reinforcing the current-limiting action. As a result, current limiting occurs at lower load currents. This type of current control, where the current reference is a function of the output voltage, results in short circuit currents that are less than rated currents, which minimizes power dissipation in the series regulator stare during load faults.
(3) Overvoltage protection. Zener reference diode A1CR5 provides a constant voltage to voltage divider A1R9, A1R30, and A1R31, which provides a fixed bias to the base of A1Q7. Transistor A1Q7 is a p part of differential amplifier A1Q7-A1Q8. A sample of the output voltage is applied to the base of A1Q8. The wiper arm of potentiometer A1R30 is adjusted so that with normal output voltage, AIQ8 is cut off due to the emitter bias across common emitter resistor A1R35. When AIQ8 is it off, the base of AIQ9 is at supply $3 / 4$ potential and AIQ9 is also cut off. If the output voltage should exceed the normal value of +4.75 volts by 115 percent ( +5.5 volts), the portion of the voltage coupled to the base of ALQ8 causes the transistor to conduct. Voltage drop across collector load resistor A134 lowers the bias on A1Q9, causing A19 to conduct also. When A1Q9 conducts, it applies a positive level to voltage divided A15R5 and A15R6 which fires silicon control rectifier A1CR2. Silicon control rectifier A14CR2 then conducts heavily and drops the rectifier output voltage to a low level.
(4) Overcurrent protection. Overcurrent protection transistor A1Q4 operates at a relatively small positive voltage level in the 4.75 -volt supply since this is the level of the output voltage being monitored. As a result, because of transistor characteristics the bias levels are insufficient to guarantee that the transistor will actually turn on if an overload condition is reached. To assure that the transistor turns on, it is supplied with a regulated negative bias from emitter follower A1Q3, which is connected to regulator Zener diode AICR1. The negatives bias supplied is approximately -11.5 volts. This same bias is supplied to the +12 -volt supply but is not required by the negative voltage regulators.
c. Turn-on and Turn-off. The regulator circuit is
automatically turned on or turned off by sequence module, A12. Turn-on is accomplished by the sequence module,, which turns on a transistor whose collector is connected to pin W of A9J4. Before turn on by the sequence module, an open circuit exists at pin W and A1Q2 cannot conduct. When the transistor in the sequence module is turned on, it provides a ground at pin W and current now flows through A1CR2 and A1CR3 and transistor A1Q2 is now driven to the conduction state. This produces a base bias for A1Q1 and collector bias for A1Q6. The base bias for Q1 causes it to conduct and produce a current source for A4Q3, which then turns on the series regulator, A4Q1 and A4Q2. Turn off is accomplished by firing overvoltage protection SCR A14CR2, thereby dropping the output voltage to near zero. Refer to paragraph 3-32 for a description of the operation of the sequence module. Diodes A1CR2 and A1CR3 provide protection for transistor A1Q2 against excessive back bias.
d. Other Regulator Circuits. The -48 -vdc regulator, $+12-\mathrm{vdc}$ regulator, and -12-vdc regulator all operate in a manner similar to the +4.75 -volt regulator. The differences are described as follows:
(1) In the -48-volt supply, transistor A3Q4 controls the turn-on in response to the switching action in the sequence module. To turn on the -48-volt supply, a bias level of approximately +15 volts is applied at pin N of A9J4 to the emitter of A3Q4. This supplies a current source to the series regulator in A6. Current overload protection is provided by current sensor A6R2 and current overload transistor A3Q1. If there is a current overload, A3Q1 is turned on, reducing the negative voltage level at the collector of A3Q1, turning on A3Q2. This turns off the regulator stage, dropping the output voltage, as described for the +4.75 -volt regulator. Normal voltage regulation is provided by differential amplifier A3Q6, A3Q7 which controls regulator control transistor A3Q3, through voltage splitter A3Q5. Transistor A3Q5 permits lower bias levels to be used than those normally available from the relatively high voltage levels which exist in the -48 -volt supply.
(2) For the -12-volt supply, turn-on control from the sequence module consists of supplying a bias of approximately +15 volts at pin V of A9J4 to transistor A2Q8, turning it on. This supplies the required current source to the -12 -volt series regulator. Other circuit operations are the same as for the +4.75 -volt supply previously described ( $b$ and c above).

## 3-32. Sequence Module A12, Detailed Circuit Description <br> fig. 8-8

The sequence module turns the complete power supply on and/or off in a predetermined manner when the AC POWER switch-indicator on the control panel is operated. Also, the failure of any one regulated do output turns off the remaining outputs in a proper sequence.
a. Input Circuit and Ac Relay Control. The 24volt dc full-wave rectifier on module A15 supplies unregulated 24 -vdc power to the normally open contacts of relay K1 on the sequence module, and to the AC POWER switch-indicator on the card reader control panel. When this switch-indicator is operated, its contacts are momentarily closed, applying the 24 vdc through diode CR21 and resistor R60 to the coil of relay K1, energizing it. The relay is then latched on by the 24 vdc through its now closed contacts, through diode CR32 and resistor R60. Thus, this relay stays energized when the AC POWER switch-indicator is released. The voltage applied to the coil of relay K1 is also applied to the base of Q1, which turns it on, causing it to conduct current. This action energizes auxiliary ac power relay, A9K1 (shown on the. regulator circuit), applying the auxiliary 115 vac power to the fans, the drive motor, the AC POWER switch-indicator lamp and the other indicator lamps.
b. Voltage Regulator. The unregulated $24-\mathrm{vdc}$ power is coupled through the contacts of energized relay K1 on the sequence module to the 15 -volt regulator. The regulator converts the unregulated 24 -volt dc power to regulated 15.0 -volt dc power. The 24 volts is applied to series regulator Q33, which acts as a variable load in series with the input voltage, varying its internal impedance to maintain the output voltage at +15.0 vdc. The series regulator is controlled in the following manner.
(1) The output voltage of the regulator is developed across voltage divider R72, R73, and R74. Capacitor C10 removes high frequency variations on this voltage. Potentiometer R73 is adjusted to obtain the required +15.0 -volt output when the overall control loop is stabilized. Should the output voltage tend to change from +15.0 volts, the voltage applied to the base of Q35 changes proportionately. The emitter of Q35 is held at a constant voltage by Zener regulator diode CR27 so that only a variation in base voltage can cause a change in collector voltage of Q35. The voltage change at the collector of Q35 is applied to the base of emitter follower Q32, which, in turn, changes the voltage at the base of Q33. This action varies the voltage drop across Q33 proportionately, returning the output voltage to the required level. For example, an increase in the
output voltage produces an increase in the voltage at the base of Q35, which results in a subsequent decrease in the voltage at the base of Q32 and Q33. This increases the voltage drop across Q33, lowering the output voltage to the required value. Transistor Q31 is connected from the base to collector of Q32 and acts as a shunt path for base current of Q32. In this manner Q31 tends to maintain a constant current source at_ the base of Q32, minimizing excessive current variations through the series regulator.
(2) For normal output currents, transistor Q34 is reverse biased by voltage divider R67 and R68 and is cut off. If the output current rises above approximately 500 ma , a sufficient voltage drop is developed across resistor R69 to overcome the back bias on Q39, causing it to conduct. This creates a shunt path for' the output current, limiting the output current to a maximum of 500 ma.
c. Turn-On Sequence. After latching relay K1 has been energized and the voltage regulator then provides the regulated +15.0 -vdc output, the regulators are turned on automatically in the following sequence: -12 $\mathrm{vdc},+4.75 \mathrm{vdc},+12 \mathrm{vdc}$, and -48 vdc . The sequence module performs this turn-on action in the following manner:
(1) -12-volt turn-on. The +15.0 -vdc output of the $+15-\mathrm{vdc}$ regulator in the sequence module is applied to voltage divider R89 and RFO The voltage at the junction of R89 and RW0 is applied to the base of Q39 whereas a reference voltage from Zener diode CR30 is applied to the emitter of Q39. The reference voltage keeps Q39 cut off until the voltage applied to voltage divider R89 and 80 reaches a level of at least 12 volts dc. This occurs after the 15 -volt regulator has been turned on and reaches 90 percent of rated output. Conduction of Q39 drives Q38 into conduction, providing the bias voltage required to operate the series regulator in the 12 -volt regulator; turning on this regulator. The collector of Q39is at approximately 24 volts dc before it is turned on and at approximately +15 volts de after it is turned on.
(2) -12-volt output sense ( 90 percent). A sample of the output of the -12-volt regulator is applied to the base of transistor Q36 of differential amplifier Q36, Q37. Voltage divider R75 and R76 connected across the output of the 15.0 -volt dc regulator provide a reference voltage to the base of Q37 The output at the common emitter of Q36 and Q37, keeps Q36 cut off until the -12-volt regulator output reaches at least - 10.80 volts. When the output of the -12 -vdc regulator exceeds the -10.80 volts, Q36 is driven into conduction. The collector of Q36 is connected to the $+4.75-\mathrm{vdc}$ regulator turn-on circuit, to control turn-on of this regulator.
(3) +4.75-volt turn-on. When Q36 is driven into conduction, its collector goes from approximately +15 volts de to -3 volts de causing Q21 to conduct. This, in turn, causes Q18 to conduct, providing the turnon bias to the series regulator of the +4.75 -volt regulator. Before conduction the collector of Q18 is at approximately 15 volts de; after conduction, it is at approximately 0.25 volt dc.
(4) +4.75 -volt output sense ( 90 percent). A sample of the output of the +4.75 -volt regulator is applied to the emitter of Q4. The base of Q4 receives a regulated reference voltage from voltage divider R9 and R10, supplied by the +15.0 -volt regulator. When the output of the +4.75 -volt regulator reaches 90 percent of rated output ( 4.275 volts), Q4 conducts, causing its collector to go from 0 volt to approximately +4.0 volts. This produces turn-on of the +12 vdc supply.
(5) +12-volt turn-on. The conduction of Q4 causes Q5 to turn on, which provides a turn-on bias to the series regulator of the +12 volt regulator. The collector voltage of Q5 is approximately +24 volts dc prior to turn-on and approximately 0.25 volt dc after turn-on.
(6) $+1 B$-volt output sense ( 90 percent). A sample of the output voltage from the +12 volt regulator is applied to the emitter of Q9. A reference voltage, provided by voltage divider R18 and R19, from the regulated +15.0 -volt regulator is applied to the base of Q9. When the output of the +12 -volt regulator reaches 90 percent of rated value ( 10.80 volts), Q9 conducts, causing its collector voltage to go from 0 volt to approximately 10 volts. This produces turn-on of the 48 -volt supply.
(7) -48-volt turn-on. The conduction of Q9 causes Q10 to turn on. Conduction of Q10 provides a current flow through voltage divider R16 and R17, causing Q8 to conduct. This conduction supplies emitter current to Q15, turning it on, and it then supplies the required bias for the series regulator of the -48 -volt supply.
(8) -48-volt output sense. A sample of the output voltage of the -48 -volt supply is applied to the base of transistor Q29, which acts as the 90 percent sensor for the -48 -volt supply. This sensor is used only in the turn-off sequence when a fault occurs.
d. Turn-Of Sequence. When the AC POWER switch-indicator on the unit is pressed to turn off power, the sequence module turns off the regulators in a sequence opposite to the turn-on sequence. The turnoff sequence is described in (1) through (10) below.
(1) -48 -volt regulator power reduction. When the AC POWER switch-indicator is depressed, the 24 volts dc from the 24 -volt de rectifier is applied through the momentarily closed contacts of the switch to the rc
pulse-forming network of C7 and R62 and pulse transformer T1. The primary of T1 forms a pulse which is coupled to the secondary, which applies this pulse to the silicon control rectifier (SCR) overvoltage turn-off diode in the -48 -volt regulator. This reduces the output of this power supply to less than 10 percent of rated output, which, in effect, turns it off. The pulse forming network produces only a short-duration single pulse upon operation of the AC POWER switch-indicator and when the switch-indicator is released, turn-off has been initiated and continues automatically. The action of this circuit has no effect during the power turn-on sequence since the -48 -volt supply is the last supply to be turned on, and the pulse forming network will have been discharged before turn-on of the 48 -volt supply is accomplished.
(2) -48 -volt, $+1 B$-volt, +4.75 -volt, 90 percent sensor inhibit. The pulse formed in transformer T1 is coupled through a second output winding to the base of Q12. Transistors Q12 and Q13 comprise a single-shot multivibrator which produces an output pulse with a duration of 80 ms . During this time duration that the single-shot is fired, it turns on amplifier Q14, which is normally cut off and which, in turn, causes Q20 to conduct. Transistor Q20 acts as a clamp, clamping the base of Q19 to a low level, through diode CR8 during the first 80 ms of the turnoff sequence. This inhibits the operation of Q19 during the sequenced shutdown accomplished by operating the AC POWER switchindicator. Transistor Q. 19 is only used to turn off the 48 -volt, +4.75 vclt and +12 -volt supplies in case of a regulator failure (e below).
(3) -48-volt output 10 percent sensor. As described in (1) above, the operation of the AC POWER switch-indicator fires the overvoltage SCR in the -48volt regulator, reducing the output voltage from this supply. A sample of the -48 -volt out put voltage is applied to the base of Q30. When the output of the -48volt supply is normal, the base voltage is sufficiently negative to keep Q30 cut off. As the output of the 48volt supply is reduced towards zero during turnoff, the base bias will become sufficiently less negative to cause Q30 to conduct, initiating power reduction of the +12 volt supply.
(4) +12-volt power reduction and -48 -volt turn-off. Conduction of transistor Q30 applies a negative voltage through diode CR19 to the base of Q27, causing it to conduct. This applies a pulse through diode CR17 of OR gate CR17, CR18 to the SCR in the overvoltage protection circuit of the +12 volt regulator. This initiates turn-off of this regulator to reduce its output voltage to less than 10 percent of rated value. The 90 percent level detector, Q9, across the output of the +12 -volt supply senses that
the output of the +12 -volt regulator drops below 90 percent of rated value and removes the turn-on bias from the series regulator of the -48 -volt regulator, completely turning off this regulator.
(5) +12-volt output 10 percent sensor. A sample of the output of the +12 -volt regulator is applied to the emitter of Q28, whereas the base of Q28 receives a reference voltage from voltage divider R50 and R51 connected across the 15.0 -volt regulated supply. Transistor Q28 is normally cut off by the high emitter voltage; however, during the turn-off sequence, when the output of the +12 -volt regulator drops to 1.8 volt, Q28 conducts, which initiates reduction of the output voltage of the +4.75 -volt supply.
(6) +4.75 -volt 7egulator output voltage reduction and +12 -volt regulator turn-off. Conduction of Q28 applies a negative voltage through diode CR15 to the base of SCR driver Q26, causing it to conduct and apply a positive voltage through diode CR13 of OR gate CR13, CR14 to the SCR overvoltage turnoff diode in the 4.75 -volt regulator. This action reduces the output of the 4.75 -volt regulator to less than 1.8 volt, in effect, turning it off. The 90 percent level detector (Q4) across the output of the 4.75 -volt supply senses that the voltage is below 90 percent of rated value. This results in Q5 being cut off, which removes the turn-on bias from the +12 -volt regulator, turning off this power supply completely.
(7) +4.75-volt output 10 percent sensor, ac power turn-off. A sample of the output voltage of the +4.75 -volt regulator is applied to the emitter of Q23 The base of Q23 receives a reference bias from the voltage divider consisting of R44 and R45 connected across the 15.0 -volt regulator. The emitter bias keeps Q23 normally cut off. When the emitter voltage drops to 1.8 during the turn-off sequence, Q23 is driven into conduction. This produces a voltage drop at the base of Q22, through diode CR10, causing it to conduct and apply a positive voltage of approximately 15 volts to base-emitter voltage divider R2 and R3 relay control amplifier Q2. Amplifier Q2 now conducts heavily, reducing the base voltage on relay driver Q1 sufficiently to turn off Q1. This removes excitation from the coil of ac power relay A9K1, turning off ac power for the drive motor, the fans, and also the AC POWER switchindicator lamp and the other indicator lamps. The now unlighted AC POWER switch-indicator lamp indicates that the ac drive motor power is turned off.
(8) -12-volt regulator voltage reduction and +4.75 -volt turn-off. The conduction of Q22 also applies +15 volts dc to the rc timer circuit of R4 and C1. During the time interval that the voltage builds up on C1, transistor Q3 is biased to be cut off and the voltage
across C1 is applied to SCR CR33. After approximately 300 ms , the voltage across CR33 builds up to $8 \pm 1$ volts dc, at which time CR33 conducts. Conduction of CR33 causes a sharp reduction in base voltage of Q3, driving it into conduction. Capacitor C 1 now discharges through Q3, and the resulting current flow through R8 to the SCR in the overvoltage protection circuit of the -12-volt regulator causes the output voltage of the regulator to drop to less than -2 volts dc. The drop in output voltage of the -12 -volt supply below the 90 percent level is sensed by the 90 percent level sensor (Q36 and Q37) connected across the output of the -12 -volt supply. This results in transistor Q21 being turned off, which removes the bias from the series regulator in the +4.75 -volt supply, completely turning off this power supply.
(9) Turn-off of -12-volt supply and power turnoff in sequence module. The discharge of capacitor C1 through transistor Q3 ((8) above) also applies a discharge current through R7 and diode CR2, into SCR CR24 across the coil of relay K1. This voltage drop is also coupled through diode CR29 to the base of Q39. This back-biases Q39, turning it off, which in turn, cuts off Q38. This removes the bias voltage from the series regulator in the -12 -volt regulator, completely turning off this power supply. The pulse applied to SCR CR24 fires this SCR, shorting out the coil of relay K1, deenergizing this relay. This removes the 24 -volt dc power from the 15.0 -volt, regulator, removing all power from the circuits of the sequence module. This completes the turn-off procedure.
(10) Transistor protection. Those level detector transistors which could be subject to relatively high reverse base-emitter voltages are protected by diodes connected between the base and the emitter. The diodes short out excess reverse base-emitter voltages.
e. Fault Sensing and Turn-Off. If the -48 -volt, + 12 -volt, or +4.75 -volt supply fails, the others must be turned off at the same time. After this is accomplished, the 12 -volt supply is turned off. If the 12 volt supply fails, the other three supplies must be simultaneously turned off within 50 ms after this failure. Turn-off is accomplished 'by means of the 90 percent sensors which sense when the output voltage of a regulator has fallen to 90 percent or less, of rated output.
(1) Should the +4.75 -volt regulator output fall to less than 90, percent of rated value, this is sensed by +4.75 -volt 90 percent sensor (Q4) which turns off, and turns off Q6, which in turn turns on Q7. The collector Q7 is reduced to near ground level, applying a negative voltage through diode CR8 to the base of Q19. This turns on Q19, providing a position
voltage through diodes CR6, CR14, mid CR18 to the 48 -volt SCR, the +4.75 -volt SCR, and the +12 -volt SCR, turning off these supplies simultaneously. Transistor Q19 is also operated by the -48volt 90 percent sensor (Q29), the +12 -volt 90 percent sensor (Q9, Q10, and Q11) or the -12 -volt 90 percent. sensor (Q36 and Q17), if any of these power supplies fail. The -48-volt SCR is operated by Q19 firing SCR CR34 across pulse-forming network C4 and R30. The output pulse is supplied to T1 for application to the SCR in the 48 -volt supply.
(2) After the -48 -volt, +4.75 -volt, and +12 volt supplies are simultaneously turned off, the -12volt supply is turned off as described in e above. If the $+15-$ volt regulator in the sequence module fails (power output drops to less than 90 percent of rated output), this is sensed by the +15.0 -volt 90 percent sensor which turns off the bias to the -12-volt series regulator. This turns off this regulator, initiating the shutdown procedure.
f. Override Timer Circuit for turn-On Circuit. As described in d above, the turn-off circuits include sensors which operate when output, voltages are below 1.8 volt dc or 10 percent of rated output, whichever is higher. In addition, the 90 percent detectors function as fault detectors if the output voltage of any regulator drops below 90 percent of rated value, as described in e above. Both of these sensors must be inhibited during the power turn-on since they would interfere with the power turn-on sequence. This is accomplished by the action of driver clamp Q24. When the 24 volt dc is initially applied to the 15.0 volt regulator to produce the regulated 15 -volt output, the +15 -volt output is applied to the emitter and base of driver clamp Q24, causing it to conduct, producing a positive voltage at its collector. This positive voltage is coupled through diodes CR20, CR16, CR11, and CR9 to -48-volt, 10 percent sensor Q30; +12-volt 10 percent sensor Q28; + 4.75 -volt 10 percent sensor Q23; and the 90 percent fault sensor line to Q19. It thus blocks diodes CR19, CR15, CR10, and CR8, preventing the 10 percent and 90 percent fault sensors from operating and turning off the power supplies. At the same time that Q24 is turned on, the +15 volts is applied to timer circuit R84 and C12. The rc time constant of this circuit is selected so that the voltage on C12 builds up to a sufficient level to turn on Q16 in approximately 1.8 second. Zener diode CR30 establishes the turn-on bias for Q16. When Q16 is turned on, it supplies base current for Q25, turning it on. This produces a positive voltage at the base of Q24 which turns off Q24, removing the inhibiting voltage from diodes CR19, CR15, CR10, and CR8. The 10 percent sensors and 90 percent fault sensor Q19 are no
longer inhibited since after 1.8 second all power has been turned on and the fault sensors should now operate.

## 3-33. Voltage Regulation for +6.2 -Volt and -6.2 -Volt Dc Power

Voltage regulator circuits are located on PC card A5 (fig. 8 -13 to produce +6.2 -volt and 6.2 -volt power for use by the receive and transmit interface circuits.
a. The -6.2-volt power is derived from the -12-volt source by Zener diode VR1 and resistor R91. Capacitor C11 minimizes the effect of switching transients on the 12-volt power.
b. The +6.2 -volt power is derived from the +12 -volt source by Zener diode VR2 in conjunction with resistor R92. Capacitor C10 minimizes the effect of switching transients on the +12 -volt power.

## 3-34. Power-On Reset Control Circuits

When power to the card reader is turned on, a reset signal is generated to clear various latches in logic assembly Al in preparation for a new card feed and read cycle. The power on reset (PRST) signal is initiated by operation of the AC POWER switch indicator on the control panel (para 3-28). When this switch-indicator is pressed, -48 volts dc is applied to the power-on reset circuit on PC card A1 (fig. 8-10 and para 3-81a). The resulting PRST signal is routed to the card feed control circuits on PC card A15.

## 3-35. Receive Interface Circuits

a. All control signals between the CCI and card reader switch between levels of 0 volt and pen ckt or 6.2 volts and +6.2 volts. These signals are generated by transmitter circuits in the CCU with high frequency components (sharp turn-on, turn-off) removed to minimize rfi problems in the cables. The receive interface circuits provide an impedance match for the CCU signals, convert them to the card reader logic format ( +4.5 volts active and 0 volt inactive), and restore the sharp turn-on, turn-off required for reliable logic operation in the card reader.
b. The receive interface circuits consist of interface receivers (E) through (K) on PC card A4 (fig. 8-12). Interface receivers (E) through (J) provide level shifting and inversion, converting inputs of 0 Volt to outputs of +4.5 volts and open circuit mt 8 to outputs of 0 volt. Four of the received inputs are active at a low level so that the outputs are active at a high level. These signals are: end of message (EOM), end of block (EOB), assigned (ASG), and select (SEL A). A fifth signal (cancel) is received on the RCAN line as a high level when active. After inversion, this results in a low level on not-function cancel line (NCAN), indicating a cancel command.
c. Interface receiver (K) differs from the other interface receivers ill that, although there is level shifting, there is no inversion. Thus, a positive received step/data acknowledge pulse input (RSDA) results in a correspond positive output pulse (SDA). An inhibit input (SINH) to this receiver is not used and wired to ground.

## 3-36. Read Station and Hopper Empty Photocell Circuits

(fig. 3-28)
a. Hopper Empty Function. The light station in the card reader mechanism contains a lamp assembly with 14 lamp filaments. An additional lamp is directed through the hopper to the hopper empty photocell. When no card is present in the hopper, the hopper empty photocell is illuminated. This produces a hopper empty signal which is converted to card reader logic levels by one of the photocell amplifiers on PC card A6 in the logic assembly. The hopper empty signal is then sent to the alarm circuits to initiate an operator's alarm.
b. Read Station Function. Of the remaining 14 lamp filaments in the light station, two are directed at the end of card and beginning of card photocells which monitor the position of the card through the read station, and the other 12 are directed at the 12 read photocells which monitor the data content in the 12 rows on the card.
(1) Read photocells. The read photocells are arranged in a line so that all 12 bits in a column are simultaneously read. The operation of a typical read photocell is illustrated in figure 3-29 for a row of holes punched in every column.
(a) The photocell, signal after conversion by one of the photocell amplifiers on PC card A6, is low when the photocell is lighted. This signal goes high when the leading edge of the card passes under the read photocells and remains high until the first column. If a hole is punched in this column in the row for that photocell, a positive pulse is produced. Similar pulses are produced for succeeding columns. After the last column, the signal remains high while the trailing margin of the card is passing under the read photocells and then goes low again after the card has passed.
(b) An indication of the presence of a card in the read station is obtained by monitoring the out puts of the 12 read photocells for a simultaneous light condition on all 12 photocells. Since there is no valid Hollerith character requiring all 12 rows in a column to be punched, the only time when all 12 photocells can be lighted is before the leading edge of the card reaches the line of read photocells and after the trailing edge of the card leaves the line of read photocells. This condition is detected by feeding all 12 data bit lines from
the photocell amplifiers on card A6 to the all-lighted detector which produces an all-lighted (LIT) signal that goes high only when all 12 read photocells are lighted at the same time (fig. 3-29). This signal is used in the data strobe control and alarm circuits as an indication of the position of a card in the read station.
(2) Beginning- and end-of-card photocells. Additional information concerning the position of the card in the read station is provided by the beginning-ofcard photocell located downstream, after the read photocells and the end-of-card photocell located upstream, before the read photocells. The position of the beginning-and end-of-card photocells is such that they are darkened when a card is in the read station and are not affected by light passing through the punched data holes.
(a) Note that six key positions of the card in its passage through the read station are shown in figure 3-30 and are designated by the letters A through F. The time at which the card is in each of these positions is also identified in figure 3-29.
(b) As a new card enters the read station, moving from right to left, the first photocell to be darkened is the end-of-card photocell. When this occurs (at time A), the end-of-card signal goes low. The end-of-card photocell remains dark as the card passes through the read station until time D when the last column has just passed under the read photocells because the spacing between the read photocells and the end-of-card photocell is equal to the distance between the end of column 80 and the edge of the card.
(c) The beginning-of-card photocell goes dark just before column 1 passes under the read photocells (at time C) and remains dark until time $F$ when the card leaves the read station. The spacing between the beginning-of-card photocell and the read photocell is equal to the distance between the leading edge of the card and column 1.
(d) The portion of the card between the beginning of column 1 and the end of column 80 is called the data field. The time when the card is in this position is monitored by a data field detector on PC card A14. The data field signal produced by the data field detector is low only when both the beginning-and end-ofcard signals are low simultaneously (fig. 3-29).
(e) An additional indication of the card position is provided by the card end detector on PC card A14. When LIT signal is low but the end-of-card signal is high, the card end signal produced by the card end detector goes high. This signal marks the time from D to $E$ when the trailing edge of the card is passing over the read photocells.


Figure 3-28. Read station and hopper empty photocell circuits, block diagram.


Figure 3-29. Read station timing diagram.

## 3-37. Read Station and Hopper Empty Photocells

The read station photocells detect the presence or absence of punched holes ill each column of the card and monitor the position of the card relative to the station. The hopper empty photocell provides an alarm indication when the last card is picked from the hopper.
a. Read Photocell. The 12 Hollerith data bits are, detected by read photocells Q1 through Q12 on subassembly A1A1 (fig. 8-9). The 12 photocells are positioned in line at the correct spacing for rows 12, 11, 10 , and 1 through 9 ), respectively, on the punched card. Light for the operation of these photocells is provided by the filaments in assembly lamp DS1 on subassembly A1DS1. When the light from these continuously lighted lamps is not blocked by the card, the individual photocells are driven into the conducting state and current that is received at the collectors from the $+4.5-$ volt supply is passed through the emitters to the photocell amplifiers on PC card A6.
b. Beginning-and End-of-Card Photocells. The position of the card in the read station is monitored by beginning of card photocell Q13 and end-of-card photocell Q14. These photocells operate from light
supplied by corresponding filaments on lamp assembly A1DS1. Both photocells are darkened (nonconducting) when the card is in the read station. The specific time when these photocells stop conducting as the card enters the read station and start conducting after it leaves the read station is used in data evaluation.
c. Hopper Empty Photocell. The cards in the hopper are monitored by hopper empty photocell A1Q1. When the hopper is empty, light from: lamp A1DS2 causes A1Q1 to conduct, producing a high level on the hopper empty line.
d. Lamps. All 14 read station lamps are connected in series with hopper empty lamp A1DS2 and voltage dropping resistor R1 across the -48-Evolt supply, and the lamps go on when power to the card reader is switched on.

## 3-38. Photocell Amplifiers

a. The photocell amplifiers convert signals from the read station and hopper empty photocells into logic signals required to operate the integrated circuits of tie card reader. There are 15 separate amplifiers (A


Figure 3-30. Card positions in read station.
through Q) on PC card A6 for the 15 photocell outputs fig. 8-14). These outputs are the 12 Hollerith data bit signals, the beginning-of-card signal (BCP), end-of-card signal (ECP), and the hopper empty (HOP) signal.
b. When light strikes any one of the 15 photocells, the photocell, acting as a switch, permits current to flow
from the +4.5 -volt supply to the photocell amplifiers. Each photocell amplifier converts the presence of current into a low output logic level ( $(0$ volt) and the absence of current into a high output logic level (+4.0 volts).
c. The read photocell amplifier outputs are not functions since they are low when holes are detected by the corresponding read station photocells, and are identified as RA 01 through RA12. To obtain true functions, these signals are inverted to produce outputs on data bit lines HOL 1 through HOL12
d. Similarly, the beginning-of-card (BCN) and end-of-card (ECN) signals produced by photocell amplifiers N and P are high when the photocell is blocked by the presence of the card in the read station. The truefunction BC and EC signals are produced by inverters Z2B and Z2a, respectively. The hopper empty (HPN) signal produced by photocell amplifier Q is also a notfunction (low when the hopper is empty). This signal is not used in its true-function form.

## 3-39. All-Lighted Detector.

The all lighted detector checks for the absence of a card at the read station by monitoring for the simultaneous detection of light at each of the 12 data bit photocells. When no card is present, low outputs are simultaneously produced by the 12 respective photocell amplifiers on PC card A6 (fig. 8-14). These low outputs enable the combination of ABD gate $\mathrm{Z5B}$ and expander AND gates Z6A, Z6B, Z7A, and Z7B. The resulting high outputs on the LIT line indicates that all read station photocells detect a lighted condition.

## 3-40. Data Field Detector

The data field detector produces an indication to determine exactly when the portion of the card containing the 80 data columns is passing under the read photocells. To accomplish this function, the end of card (EC) and beginning of card (BC) signals from the photocell amplifiers of PC card A6 are applied to AND gate Z20A on card A14 which produces a low output only when both inputs are low (fig. 8-22). Since the Z20A output is low only when both inputs are low, the data field signal produced by Z20A goes low just before column 1 and remains low until; after the end of column 80 fig. 3-30.

## 3-41. Card End Detector

The card end detector is used to detect the time that the portion of the card between column 80 and trailing edge is passing under the read photocells. This function is performed by AND gate Z14B on PC card A14 (fig. 822). The AND gate monitors the all-lighted (LIT) signal from the all-lighted detector
on PC card A6 and not-function end of card signal (NEC) which is derived by inverting end of card signal (EC) from the photocell amplifiers on PC card A6. Figure 3-29 illustrates that these signals are both low during the required time since NEC signal goes low after column 80 and the LIT signal is low up to the trailing edge of the card. The high end of card output (EOC) of AND gate Z 14 B is also applied to AND gate Z12A where it enables a C5 (count of 5) pulse from the timing counter is the data strobe control circuits to pass through to the cycle complete (CC) line. This pulse indicates that the card has been completely read and that the next card may be picked from the hopper.

## 3-42. Card Feed Control Circuits

(fig. 3-.31)
The card feed control circuits contain a card feed start control circuit which controls the generation of the pick command for the card feed solenoid and a card feed stop control circuit disables card feed operation by the card feed start control circuit when required. In addition, a ready control circuit generates a ready signal for transmission to the CCU unless the card feed start control circuits are being operated in a local mode which would exclude CCU control of the card feed.

## 3-43. Card Feed Start Control Circuit

The card feed start control circuit controls the operation of the pick solenoid in the card reader mechanism. The solenoid is allowed to pick a single card when the SINGLE FEED switch-indicator on the control panel is pressed. When the LOCAL TEST switch-indicator is
pressed, the solenoid is repeatedly activated as each card is read. When the START switch-indicator is pressed, the solenoid is activated only upon a step or command from the CCU for a new data block. Each of the three switch-indictors performs its function only if the card reader is in a stop condition at the time the switchindicator is pressed. Normally, a stop condition is achieved by pressing the STOP switch-indicator, otherwise a stop condition is initiated automatically by any one of a number of alarm conditions detected by the various alarm circuits.

## 3-44. Single Feed Operation

a. When SINGLE FEED switch-indicator Z4 is pressed, a high level ( 4.5 volts de) is applied to the single feed open (SFO) line, conditioning AND gate Z21A on PC card A16 (fig. 8-24), Since this AND gate monitors the stop signal (STP), it is inhibited if the card reader is not in a stop condition. When Z21A is enabled, the high output sets debounce latch Z18, which removes the effects of switch bounce from the signal. The resulting high level output conditions AND gate Z21B and also activates OR gate Z26B. Prior to activation of Z26B, the high level at the Z26B output clears flip-flop) Z25.
b. The action described in a above, results in a single start pulse from AND gate Z26A to latch Z16 to remove the stop condition in the stop control circuit. The start pulse also sets flip-flop Z13 through AND gate Z21B.


Figure 3-31. Card feed control circuits, block diagram.

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c. The resulting high output of $Z 13$ on single feed line SF, lights SINGLE FEED switch-indicator Z4 by activating a lamp driver on PC card A3.
d. Single feed signal SF also enables AND gate Z9B unless the card reader has been assigned by the CCU. In this case, the assigned line ASG is inverted to a low level by inverter Z1OA to disable AND gate Z9B. This prevents automatic card advance under control of the SINGLE FEED switch-indicator; however, card advance can still occur under control of the step data acknowledge interface line SDA from the CCU, gated through AND gate Z4A.
e. Assuming that the card reader is not assigned to the CCU, ANT) gate Z9B produces a high level when SINGLE FEED switch-indicator Z4 is pressed. This signal activates OR gate ZSA which feeds a low level to AND gate Z6A. If the other two conditioning inputs to ZGA are low, a low level is produced on advance solenoid driver line ASD. The ASD signal activates solenoid driver Q1, Q2, Q3 on card A1 (para 3-81), This solenoid driver then supplies a ground level to energize the pick solenoid in the card reader mechanism.
f. One of the other two conditions for enabling AND gate Z6A to produce the ASD output is a low level on the stop line from the stop control circuit. This insures that a new pick command is not generated if the card reader is still in the stop state. The second condition is a low level on not end of card line NEC. This insures that a new pick command is not, generated if the previous card is still in the read station, blocking the end of card photocell. Also, this removes the ASD signal from the solenoid driver once the new card has reached the read station.
g. As soon as the card has passed through the read station, a cycle complete (CC) pulse is generated. This clears flip-flop Z13, terminating the SF signal. Thus, SINGLE FEED switch-indicator Z4 is extinguished; AND gate Z9B1becomes disabled; and a new pick command cannot be generated until the next, time SINGLE FEED switch-indicator Z4 is pressed. Even if Z 4 is held ill the depressed position (so that latch Z18 remains set.) AND gate Z21B does not set flip-flop Z13 again because flip-flop Z25 must be cleared before a new enabling pulse is supplied to Z2i.13. Flip-flop Z25 is not cleared until SINGLE FEE,) switch-indicator 74 is released. At that time, the +4.5 -volt level is switched back to the SFC line, clearing latch Z18 and, in turn, deactivating OR gate Z26B. The high output of Z26B can then clear flip-flop Z25.

## 3-45. Local Test Operation

a. When LOCAL TEST switch-indicator $\mathrm{Z5}$ is pressed, a high level is switched to the local test open (LTO) line conditioning AND gate Z24A on PC card A16 (fig. 8-241). This gate also monitors the stop and not assigned (NASG) signals. Both of these signals are high if the card reader is in a stop condition and has not been assigned by the CCU. The resulting high output of Z24A sets debounce latch Z27.
b. The high output of Z 27 activates OR gate Z2613, resulting in a pulse from ANI) gate Z26A in the same way as for single-feed operation. This pulse is fed to the stop control circuit to remove the stop condition.
c. In addition, the high output of Z27, in turn, sets latch Z23 to produce a high level on logic test line LT. This signal activates OR gate ZSA to cause the generation of a pick command in the same way as in single-feed operation. The solenoid advance signal (ASD) remains high until the new card has entered the read station. At that time, not end of card signal NEC goes high, disabling ANI) gate Z613 and terminating the ASD signal.
d. Since the LT line remains high, a new pick command is generated as soon as the card has left the read station. At that time, the NEC signal goes low again, enabling AND gate Z6A to place a high level on line ASI). As long as the LT line is high, this line activates a lamp driver on PC card A3 to energize LOCAL TEST switch-, indicator Z5 on the control panel.
e. Whenever the stop control circuit. produces a stop signal at the output of OIR gate Z7A, this signal is fed back to clear latch Z22, switching off the local test, mode. When remote operation is initiated by operation of START switch-indicator Z7, a high level is fed from the Z22A output of latch Z22 to clear latch Z23, thereby preventing local test operation from being selected.

## 3-46. Remote Operation

a. To allow the card feed function to be remotely controlled, the operator presses START switch-indicator Z7 on the control panel. This transfers a high level from line SC to line SO. The SO signal enables AND gate Z24B if the card reader is in a stop condition (stop signal from OR gate Z7A is high). The resulting high output of AND gate Z2413 sets latch Z28. The high output of Z28 activates OR gate Z2613. This results in the removal of the stop condition by the stop control circuit in the same way as for single feed and local test. operation.
b. The high output of latch Z28 also sets latch Z22 which, in turn, supplies a high level from the Z22A
output to hold local test latch Z23 cleared. In addition, the low level at the Z22B output conditions AND gates Z11A and Z11B. As long as the card reader has not yet been selected by the CCU, the SET, A line from tile receive interface circuits is low. This conditions AND gate Z11A.
c. Finally, if the card reader is in the ready state, the not ready signal from OR gate Z 713 in the ready control circuit is low. This enables AND gate Z11A to produce a high level on line DSG. The DSG line activates a lamp driver on PC card A3 to energize the green indicator portion of START switch-indicator $\mathrm{Z7}$. The white portion is not energized until the SEL A goes high. This disables AND gate Z11A and is inverted to a low level by inverter Z8B to condition AND gate Z11B. If the card reader is still in a ready state (Z7B output low), AND gate Z11B is disabled. This results in a high level on the DSW line which activates another lamp driver on PC card A3 to energize the white indicator portion of START switch-indicator Z7.
d. The actual solenoid drive impulse for the pick solenoid is not generated until a step/data acknowledge (SDA) signal is received from the CCU. This results in a high level on the SDA line from the receive interface circuits which conditions AND gate Z4A. If the select signal from the CCU is also active, the high level on the SEL A line conditions AND gate Z4A which is enabled to produce a high output on gated step line GS. This signal activates OR gate Z8, producing a low level which goes to AND gate Z6A to generate the ASD solenoid drive signal. As for single-feed and local test. operation, the ASD signal remains high until the picked card enters the read station.

## 3-47. Card Feed Stop Control Circuit

The card feed stop control circuit generates the stop command for the card feed control circuit. Normally, the stop command is removed by a start pulse from the card feed control circuit when one of three card feed switchindicators is operated (SINGLE FEED Z4, LOCAL TEST Z5, and START Z7). In the case of SINGLE, FEED switch-indicator Z4, the stop command is renewed as soon as the picked card passes through the read station. In the case of switch indicators $\mathrm{Z5}$ and $\mathrm{Z7}$, the stop command is normally not renewed until STOP switchindicator Z6 is pressed.
a. The stop command signal is controlled by OR gate Z7A on PC card A16 (fig. 8-24). Whenever the output of Z7A goes high, AND gate Z6A in the card feed control circuit is disabled, thereby preventing a new card from being -picked. The Z7A output is also passed through buffer Z6B to the STP line. This activates a lamp driver on PC card A3 which energizes STOP switch-indicator Z6 on the control panel.
b. If the alarm stop circuits on PC card A15 detect an alarm stop or operator alarm condition, a stop command is produced. Therefore, a low level on not alarm stop line NAST or not operator alarm line NOA is inverted by inverter Z3A or Z3B, respectively, to activate OR gate Z7A.
c. The third input to OR gate Z7A is controlled by AND gate Z15A which is enabled only if both latches Z14 and Z16 provide low inputs. Normally, when power is first turned on to the card reader, power on reset line PRST goes high. This activates OR gate Z20B to provide a high output which is passed through OR gates Z17B and Z20A to clear latches Z14 and Z16. Thus, the latches provide low levels to AND gate Z15A, causing a stop condition. The same effect is obtained if RESET switch S1 on the front panel of the logic assembly is pressed when the card reader is not assigned to the CCU. At that time, AND gate ZL9A is conditioned by a low level on assigned line ASG and receives a low level at its second input on reset line RSTO from the RESET switch. The resulting high output of AND gate Z19A activates OR gate Z201B, causing both latches to be cleared.
d. To remove the stop command, one of the three card feed switch-indicators be operated (SINGLE FEED Z4, LOCAL TEST Z5, and START Z7). In either case, a single positive start pulse is produced at the output of AND gate Z26A. This is fed directly to the set side of latch Z16 and through OR gate Z17B to the clear side of latch Z14. The resulting high output from Z 16 disables AND gate Z15A, removing the stop condition even though a low level is still being received from latch Z 14 .
e. Latch Z14 does not become set until the first advance solenoid drive pulse (ASD) is produced by the card feed control circuit to pick the first card. This negative pulse enables AND gate 72A if the hopper is not empty (hopper empty line HPFE from the hopper empty photocell amplifier is low) and if the stacker is not full (stacker full line STFO from the stacker full sensing switch on the card reader mechanism is high). The high level on the STFO line is provided by resistor R1 on PC card A15, since the sensing switch is open when the stacker is not full. This high level is inverted by inverter Z2B on PC card A16 to enable AND gate Z2A. The resulting high level sets latch Z14.
f. After the card that is picked completes its passage through the read station, a positive cycle complete pulse (CC) is received from the card end detector on card A14. This signal clears latch Z14 again. However, the stop condition does not return unless latch Z16 is also cleared. Normally (unless STOP switch-indicator Z 2 is pressed) this occurs
only if the SINGLE FEED switch- indicator Z4 is pressed. In that case, the CC pulse enables AND gate Z9A which is conditioned by the high level on singlefeed line SF. The resulting high output of Z9A is passed through OR gate Z20A to clear latch Z14. This restores the stop condition, thereby preventing more than one card from being fed as a result of a signal switchindicator operation.
g. However, in case of card feed initiated by LOCAL TEST switch-indicator Z5 or START switchindicator Z7, card feed normally continues automatically (with the limitation of CCU control) in case of START Z7. Card feed call be stopped at any time by pressing STOP switch indicator Z6. This connects a high level to stop line STOP which clears latch Z1G; however, the stop command is delayed until the card being read, if any, has passed through the read station. At that, time, cycle complete signal CC clears latch Z14 and low levels are again available at both inputs to AND gate Z15A.
h. A stop command is automatically generated if the hopper becomes empty. At that time, hopper empty signal HPE, goes high,, activating OR gate Z20A which clears latch Z16. Then, when the card being read passes the read station, the CC pulse clears latch Z14 and the stop command is given.
i. The signal at the output of latch Z14 normally goes high when a pick command is given (line ASD goes low) and returns to a low level as the cared that has been picked leaves the read station. Thus, tile Z14 output indicates a complete card pick-read cycle and is designated CYCL.

## 3-48. Ready Control Circuit

a. The ready signal is controlled by OR gate Z7B on PC card A16 (fig. 8-24). This OR gate becomes activated if any of the following three conditions exist:
(1) A card feed stop condition as indicated by a high level from the card feed control circuit.
(2) A local test card feed condition as indicated by local test signal LT from the card feed control circuit.
(3) A signal feed condition (card being read because of operation of SIGNAL FEED switch-indicator Z4 when in not assigned mode) as indicated by a high level from AND gate Z9B in the card feed control circuit.
b. When none of the inputs to OR gate Z7B is high, a low output is produced. This is inverted to a high level on RDY line by inverted Z10B. The RDY output is fed to the transmit interface circuits for transmission to the CCU.

## 3-49. Hollerith-to-ASCII Converter, Block Diagram

 (fig. 3-32)a. Hollerith Decoding. To convert the 64 characters encoded in 12 Hollerith data bits into the equivalent characters encoded in 8 ASCII data bits, it is first necessary to decode each of the 64 Hollerith characters codes. This is accomplished in two stages as described in (1) through (4).
(1) The characters represented by the 12 Hollerith bits are converted to a two-bit octal code, in which each octal digit is represented by the $8 \times 8$ matrix shown in table 3-1. In this matrix, one octal digit specifies a column and the second octal digit specifies a row.

## NOTE

The card reader has been modified to use the Federal standard FIPS-14 card code. Text reference to Hollerith are applicable to the FIPS-14 code.

Table 3-1. Octal Decode Matrix

| Row | Column |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | Space | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 1 | 8 | 9 |  | \# | \# |  | = | " |
| 2 | 0 | 1 | S | T | U | V | W | X |
| 3 | Y | Z | 1 |  | \% |  | > | ? |
| 4 | - | J | K | L | M | $\overline{\mathrm{N}}$ | 0 | P |
| 5 | Q | R | $\overline{0}$ | \$ | * | ) |  | $\wedge$ |
| 6 | \& | A | B | C | D | E | F | G |
| 7 | H | 1 | J |  | < | $($ | + | ! |

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Figure 3-32. Hollerith to ASCII converter, block diagram.
(2) Each of the 64 positions on the matrix is specified by a different combination of the two octal digits, therefore, the $8 \times 8$ matrix specifies the octal coding for the 64 Hollerith characters. Once the Hollerith code is converted to two octal digits, each of the 64 characters can be decoded by monitoring its specific column-row combination.
(3) when the Hollerith code for a specific character is read from the punched card, the Hollerith code is converted to the corresponding octal code specified in table 3-1 by a Hollerith to octal converter. The octal us then decoded by a decoder matrix and one of 64 lines representing the punched character is activated.
(4) Theoretically, the 12-bit Hollerith code could be converted into any arbitrary octal code other than the one in table 3-1; however, this one is used because it permits relatively easy conversion as described ill paragraph : 3-50.
b. ASCII Encoding. Once the 64 Hollerith characters are decoded onto 64 separate lines, the conversion to air eight-bit ASCII code can be performed. This is done in two stages ((1) through (4) below) which are the reverse of the decoding process.
(1) First, the 64 characters are encoded as two octal digits represented by eight lines each. Actually. there are 15 physical lines; the eighth row condition is the absence of the other seven. The octal digits (designated F and G ) for each character can be represented by the ASCII matrix in table 3-2. The columns in this matrix are arbitrarily designated 4 through 11.
(2) The $8 \times 8$ ASCII matrix in table 3 -2 is obtained by using the binary of the first three bits in the ASCII code to specify one of eight rows ( 0 through 7 ) and tire binary value of the next four digits to specify one of eight columns (4 through 11). (The eighth ASCII bit is a parity bit and has no effect on the character selected.) Therefore, the ASCII character L is coded as

11001100 in bits 8 through 1, respectively. Bits 7 through 4 (1001) spec if column G9 find hits 3 through 1 (100) specify row F4.
(3) The circuit which converts the 64 separate lines to the octal row and column code is called an encode matrix. This circuit activates a different combination of a column line and a row line for each of the 64 characters.
(4) Once the conversion to octal coding is complete, the two-digit octal code is converted into its ASCII equivalent by encoding each octal digit into its binary equivalent as specified in figure 3-4. The parity bit is made active or inactive as necessary to make the total sum odd.

## 3-50. Hollerith-to-Octal Converter

The 12 Hollerith bits read from the card are converted to a two-digit octal code by the Hollerith-to-Octal converter. One octal digit determines the row in the Hollerith matrix and the second octal digit determines the column.
a. To demonstrate how the Hollerith 12 -bit code is broken down for presentation in a two-digit octal code, the $8 \times 8$ matrix shown in able 3-1 s represented by its Hollerith equivalent in able 3-3. Table 3-3 lists the Hollerith bits punched for each character in the matrix. For example, the character $S$ in row 2, column 2 is coded by Hollerith bits 2 and 10 (fig. 3-4).
b. Note that table 3-3 shows that, in general, the column select octal digit has the same value as the digit punched in Hollerith bits 1 through 7. The only exceptions are that in rows 1,3,5, and 7, Hollerith bit 9 is used in place of bit 1 and in rows 5 and 7, Hollerith bit 10 is used in place of bit 2 .
c. Similarly, each of the eight rows is generally characterized by a specific code combination in Hollerith bits 8 through 12; therefore, row 0 contain no punches in. any of these bits, row 1 contains a punch in bit 8 , row 2 contains a punch in bit 10, row 3 contains a punch in bits 8 and 10, row 4 contains

Table 3-2. ASCII Matrix Chart


Note: Encircled characters will cause ASClI data bit 6 to also be transmitted as a " 1 ".

Table 3-3. Hollerith-to-Octal Matrix, Hollerith Coding

| Row | Column |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 67 |
| 0 | 0 | 1 |  | 3 | 4 |  |  |  |
| 1 | 8 | 9 | $(8-3)$ | 8-3 | 8-4, | $85$ | (8-9) | $(8-7)$ |
| 2 | 10 | 10-1 | 102 | 10-3 | 10-4 | $10-5$ | 10-6 | $10-7$ |
| 3 | 10-8 | 10-9 | $\binom{10-8}{2}$ | $\begin{gathered} 10-8 \\ 3 \end{gathered}$ | $\begin{gathered} 10-8 \\ 4 \end{gathered}$ | $\binom{10-8}{5}$ | $\binom{10-8}{6}$ | (10-8) |
| 4 | 11 | 11-1 | 11-2 | 11-3 | 11-4 |  | 11-6 | 11-7 |
| 5 | 11-8 | 11-9 | 11-10 | $\begin{gathered} 11-8 \\ 3 \end{gathered}$ | $\begin{gathered} 11-8 \\ 4 \end{gathered}$ | $\binom{11-8}{5}$ | $\binom{1-8}{6}$ | (1-8 |
| 6 | 12 | 12-1 | 12-2 | 12-3 | 12-4 | 12-5 | 12-6 | 12-7 |
| 7 | 12-8 | 12-9 | 12-10 | $\begin{gathered} 12-8 \\ 3 \end{gathered}$ | $\begin{gathered} 12-8 \\ 4 \end{gathered}$ | $\left(\begin{array}{c} 12-8 \\ 5 \end{array}\right.$ | $\binom{12-8}{6}$ | (12-8 |

a punch in bit 11, row 5 contains a punch in bits 8 and 11, row 6 contains a punch in bit 12, and row 7 contains a punch in bits 8 and 12. The only exceptions to these rules are in column 1 where the punch in bit 8 is
replaced by a punch in bit 9 for rows $1,3,5$, and 7 .
d. The characteristics of the Hollerith-to-Octal matrix described in b and c above are used as the basis
for developing the column and row selection digits (paras 3-51) and 3-52).

## 3-51. Hollerith-to-Octal Column Selection

a. As described in paragraph 3-50f, the column select. octal digit ]has the same value as the digit punched in Hollerith bits 1 through 7. In addition, the column select octal digit assumes a value of 1 whenever Hollerith bit 9 is punched. Also, the column select octal digit assumes a value of 2 when either Hollerith bits 10 and 11 or 10 and 12 are punched (rows 5 and 7 ), even though the Hollerith bit 2 is not punched.
b. The octal digits are developed in not-function form on PC card A8 (fig. 8-16) by routing Hollerith bits 3 through 7 to corresponding inverters (Z6B, Z6A, Z9A, Z913, and Z24A) for octal bits 3 through 7. Octal bit 1 (COLUMN 1) is produced as a low level signal by OR gate Z22B when either Hollerith bit 1 or bit 9 is high. Octal bit 2 (COLUMN 2) is produced as a low level signal by OR, gate Z3A either when Hollerith bit 2 is high or when the $10(11+12)$ signal produced by AND gate Z 13 B is high.
c. The $10(1+12)$ combination is used only for the $\bar{O}$ character ( 10 and 11) and the $\%$ character ( 10 and 12). This combination is obtained by feeding Hollerith bits 11 and 12 to OR gate Z17B and then feeding the Z17B output to AND gate Z13B together with Hollerith bit 10 ; therefore, if Hollerith bit 10 is high at the same time as either bit 11 or 12, Z13B is enabled and OR gate Z3A produces a low output.
d. Octal bit 0 (COLUMN 0 ) is activated when no hole is punched in Hollerith bits 1 through 7. This is detected by AND gate Z10B which monitors the outputs of OR gates Z7B, Z11A, and Z15A in the invalid character detector (para 3-66). These outputs are all low when Hollerith bits 1 through 7 are all low. When this happens, $\mathrm{Z10B}$ is enabled to produce a low output on the octal 6 (COLUMN 0) line.

## 3-52. Hollerith-to-Octal Row Selection

a. The row select octal digit is considered to be the more significant digit of the two-digit octal number which specifies each character. This digit is developed in two stages. First, the row selection is encoded in three binary bits, and then the binary value is converted to its octal equivalent.
b. Row select binary bit 1 is true for rows $1,3,5$, and 7 since the corresponding octal digits $(1,3,5,7)$ are coded in binary as 001, 011, 101, and 111. The characters in these four columns of the matrix are identified by a punched hole in either bits $8,9,10$, and 11 , or 10 and 12. The 10 and 11 , and 10 and 12 combinations are used only for the $\bar{O}$ and $\begin{gathered}\text { characters }\end{gathered}$ and are developed by AND gate Z13B as described in
paragraph 3-51C Therefore, the Z13B output (10 $(11+12)$ ) is applied to OR gate Z22A together with Hollerith bits 8 and 9 . If any of the inputs to Z22A goes high, Z22A produces a low 8 output. This is inverted to true-function form by inverter Z24B.
c. Row select binary bit 2 is true for columns 2, 3, 6 , and 7 since the corresponding octal digits $(2,3,6,7)$ are coded in binary as 010, 011, 110, and 111. The' characters in these four columns of the matrix are characterized by a punch in bit 10 if neither bit 11 nor 12 is punched or by a punch in bit 12.
(1) Hollerith bit line 12 is routed directly to OR gate Z17A to produce a high output on octal row 2 whenever bit 12 is punched. This is inverted to not function form by inverter Z21.
(2) The other input to Z17A is controlled by AND gate Z13A which monitors bit 10 and the output of inverter Z21B. The Z21B signal is low when either bit 11 or 12 is punched since these bits are fed to OR gate Z17B which controls the input to Z21B. AND gate Z13A activates row 2 only when bit 10 is punched without bit 11 or 12.
d. Row select binary 4 is true for columns $4,5,6$, and 7 since the corresponding octal digits $(4,5,6,7)$ are coded in binary as 100, 101, 110, and 111. The characters in these four columns of the matrix are characterized by a punch in Hollerith bit 11 or 12. Binary bit 4 is controlled by OR gate Z17B which pro duces a high output on octal row 3 when either bit 11 J or 12 is punched. This is inverted to not-function form by inverter Z21B.
e. The three row select binary bits are converted to octal form by eight decoder AND gates Z25 through Z28. Each AND gate monitors a different combination of the three binary bits. Each possible combination is monitored by a separate AND gate so that only one AND gate is enabled at any one time. The enabled AND gate produces a low output representing the selected row number while the other AND gates produce a high output. The value of the row is equal to the sum of the not-function input binary digits. AND gate Z27B, which receives 1, 2, and 4, produces a low output for row $3(1+2=3)$ when all three inputs are low.

## 3-53. Decode Matrix

a. The decode matrix decodes the two octal digits from the Hollerith-to-octal converter on 64 output lines representing the 64 characters specified by the 64 possible combinations of the two octal digits table 3-1. The matrix consists of 64 decoder AND gates each of which monitors a different combination of the two octal digits. The 64 decoder AND gates are located on identical PC cards A9 and A11 (figs. 8-17) and 8-19).
b. PC card A9 contains 32 AND gates which decode the characters in the first four rows of the matrix, and PC card A11 contains 32 AND gates which decode the characters in the last four rows of the matrix.
c. The And gate which receives a low level at both its row select and column select inputs is enabled to produce a high level output representing the selected character. All other AND gates specifying the other 64 characters are inhibited since any row-column combination can satisfy only one AND gate.
d. For example, if the character T is punched on the card, the Hollerith-to-octal converter activates column 3 and row 2 of the matrix as shown in table 3-1. and the COLUMN 3 and ROW 2 input lines to PC card A9 are both low. The only AND gate which monitors both these lines is AND gate Z18B on PC card A9; therefore, only $\mathrm{Z18B}$ is enabled to produced a high output.

## 3-54. Encode Matrix

a. The encode matrix encodes the 64 characters form the decode matrix into two octal digits representing the row and column of the $8 \times 8$ portion of the ASCII matrix (table 3-2). The encode matrix consists of a set of a OR gates located on identical PC cards A10 and A12 figs. 8-18 and 8-20.
b. Each of the 64 characters (except those in row 0 and column 0 ) is routed to two OR gates, one of which defines the column digit if the output octal code and the other of which defines the row digit. The OR gates controlling columns G4, G5, G6, and G7 are located on PC card A10, and the OR gates controlling columns G8, G9, G10, and G11 are located on PC card A12.
c. In addition, OR gates are provided for each of rows F1 through F7 on both PC cards A10 and A12. The respective row outputs are wired together externally to the two card. For example, the output of row 1 OR gate Z11 on PC card A10; therefore, if either A10Z11 or A12Z11 is activated, a high output is produced on the common row F 1 output line to the octal-to-ASCII converter. No OR gate is used for row F0 since this row is assumed to be active whenever the other rows are inactive.
d. As an example of encode matrix operation, assume that the characters T is punched on the card. As indicated in table 3-2 this character is defined by the intersection of row F4 and column G10 in the ASCII matrix. Therefore, the line representing this character is routed to OR gate Z2B on PC card A12 which controls the line representing column G10 and to OR gate Z14 which controls the line representing row F4. The high
level on the character T line causes both Z2B and Z14 to produce high outputs.

## 3-55. Octal-to-ASCII Converter

The row and column octal digits from the encode matrix are converted into the corresponding eight-bit ASCII code by the octal-to ASCII converter. The eight ASCII bits consist of seven bits ( 1 through 7 ), which define the characters and one parity bit.

## 3-56. Generation of ASCII Bits 1 Through 7

a. ASCII data bits 1,2 , and 3 are defined by rows 0 through 7 of the matrix. The octal row selection digit from the encode matrix is converted into the equivalent three-bit binary code on ASCII data bit lines 1, 2, and 3 by three expanded OR gates on PC card A13 (Z25A, Z27A; Z25B, Z27B; Z22A, Z23A) as shown in figure 821. The data bits 1,2 , and 3 have the binary value of 1 , 2 , and 4 , respectively. Each row selection digit are is encoded by feeding it to the OR gates which control the binary equivalent lines, For example, F6 converts to 110 (binary 6) on lines 3,2 , and 1 of the ASCII output. When none of the seven row select digits are activated, a row FO selection is indicated. In this case, all the three binary output lines remain low (000).
b. ASCII data bits $4,5,6$, and 7 are defined by columns G4 through G11 of the matrix and the column selection from the encoded matrix is converted into the equivalent four-bit binary code as specified by table 3-2. This is accomplished by feeding the column G4 through G11 lines to four sets of expanded OR gates on PC card A13 which control data bits 4,5, 6, and 7. To allow an arithmetical conversion, the binary value of these four data bits is designated $1,2,4$, and 8 , respectively. Each column selection is encoded by feeding it to the OR gates which control the binary equivalent lines. For example, the column G10 signal is fed to the OR gates which control data bits 5 (binary 2 ) and 7 (binary8), and the G10 signal is converted to binary bits 2 and 8 ( $2+8=10$ ); therefore, whenever the punched characters is in column G10, a high output is produced in the data bit 5 and 7 lines (ASC5 and ASC7). Table 3-3. 1 shows the ASCII data bits generated by an input on each row and column of the encode matrix. Inputs on both a row and a column will produce the proper ASC11 data bits for the character. For example; inputs on both row F3 and column G8 produces ASCII data bits 1, 2, and 7 ( 1000011 ) which is the ASCII code for the character C.
c. The O and O characters are unique in that these are the only characters that develop both ASCII data

Table 3-3.1 ASCII Encode Matrix

| Input on Rows | Generates <br> ASCII Bits <br> (none) | Input on <br> Column | Generates <br> ASCII Bits |
| :---: | :---: | :---: | :---: |
| F0 | G4 | 6 |  |
| F1 | 1 | G5 | 4,6 |
| F2 | 2 | G6 | 5,6 |
| F3 | 1,2 | G7 | $4,5,6$ |
| F4 | 3 | $G 8$ | 7 |
| F5 | 1,3 | G9 | 4,7 |
| F6 | 2,3 | G10 | 5,7 |
| F7 | $1,2,3$ | G11 | $4,5,7$ |

${ }^{\text {a }}$ Inputs to columns G1, G2, C3, G12, G13, G14 and G16 wired to ground.
bits 6 and 7 as a "1". As described in paragraph 3-51c when the 10 and 11 or 10 and 12 combinations are punched in the card AND gate Z13B on PC card A8 (fig. $8-16$ is high. This high is applied to terminal 6 on PC card A8 and connected to OR gate Z11B on PC card A13 fig. 8-21 through terminal J on PC card A13. The high output of OR gate Z11B thus develops a high output on ASCII Bit 6. The remaining ASCII bits for these two characters are developed in a normal manner as described in b above.

## 3-57. Generation of ASCII Parity Bit

a. The parity bit is developed by determining _ whether the sum of the other seven data bits is odd or even. This determination is made in two stages. First, a determination as to whether the sum of data bits 1,2 , and 3 is odd or even and as to whether the sum of data bits $4,5,6$, and 7 is odd or even. Then, these two sums are compared to determine if the total sum is odd or even.
b. There are four possible combinations of data bits 1,2 , and 3 involving an odd sum (001, 010, 100, and 111). These combinations are represented by the octal row select digits F1, F2, F4, and F7, therefore, if the character punched on the card is in rows F1,

## Change 6 3-38

F2, F4, and F7 of the ASCII matrix, the sum of data bits F1, F2, and F3 is odd. This condition is detected by routing the row F1, F2, F4, and F7 lines to expanded OR gate Z18A-Z19A on PC card A13 (fig 8-21). If any of the lines are high, the OR output is law, indicating an odd sum
c. The parity detection for data bits $4,5,6$, and 7 is performed in a similar manner and the combinations of these bits involving an even sum are represented by column select digits G5, G6, G9, and G10. If the character punched on the card involves an even sum of data bits $4,5,6$, and 7 , a high level is applied to the OR gates $\mathrm{Z} \% 6 \mathrm{~B}, \mathrm{Z1813}$, and $\mathrm{Z19i}$, and a low level output is produced at the output of $Z 18 \mathrm{~B}$.
d. The odd and even sum outputs for the two sets of data bits are fed to the comparator circuit formed by ANI gates Z9A and Z13A, and OR gate Z13n for final parity evaluation. AND gate Z9A receives both high inputs only if the bit $1,2,3$ sum is odd and the bit 4,5 , 6,7 sum is odd and AND gate Z13A receives both low inputs only if the bit $1,2,3$ sun is odd and the bit $4,5,6$, 7 sum is odd. In either case, a high output is routed into OR gate Z131B on the parity bit line, indicating that the sum is odd. If the input sums are both even, or both odd Z9A and Z1 3A are both disabled, and Z13Bi produces a high output on the parity bit line to keep the total bit sum odd.

## 3-58. Data Strobe Control Circuits (fig. 3-33)

A data strobe pulse is generated each time a card column of data is available in the data register.
a. To insure that data strobe pulses are generated at the proper time, the date strobe control circuits are synchronized to the movement of the card through the read station. This is accomplished by using the timing signal from the timing gear in the card reader mechanism. The timing signal is a sine wave at eight cycles per column of the card (approximately a 300= sec period). The timing signal is fed to a clock pulse generator on PC card A15 nowhere it is converted to clock pulses at 16 pulses per column of the card. If variations in operation of the motor in the card reader mechanism cause the card to slow down or speed up slightly, the timing gear speed follows proportionately because it is also driven by the motor; therefore, the clock pulses are always generated at 16 pulses per column.
b. The width of the holes punched ill each column of the card corresponds to approximately 10 clock pulses, and the space between holes corresponds to approximately 6 clock pulses. The data is gated into the data register at the fifth clock pulse after the start .of the hole by a sample pulse and is strobed by the data strobe at the eighth clock pulse (fig. 3-34). To control data sample and data strobe generation at the proper time,
the clock pulses are counted by a 16 -count timing counter on PC card A14. This counter is cleared to a count of 0 at the beginning of each column and reaches a count of 15 (binary 1111 ) prior to the zero count.
c. The time that passes between the appearance of the card leading edge at the read photocells and the leading edge of the first column is measured by 42 clock pulses, which comprise two complete 16 count cycles of the timing counter plus 10 counts. To insure that the timing counter begins the first column on the count of 0 , it is preset to the count of 6 at the leading edge of the card (fig. 3-35), therefore, the timing counter recycles after the first 10 counts and recycles twice again before the leading edge of the first column is reached.
d. The timing counter is held preset to 6 by a LIT signal from the all-lighted detector when no card is present over the read photocells. As soon as the leading edge of a card reaches the 12 read photocells, the preset condition is removed from the counter and the counter is allowed to advance.
e. To insure that the timing counter is cleared to 0 at the start of each hole if the card slips slightly and the timing is thrown off, the 12 data bits from the photocell amplifiers are fed to a sync generator on PC card A14. This circuit produces a sync pulse which goes high as soon as any one of the 12 data bit photocells is lighted. All columns of valid information, except the space character, on the card have at least one hole punched. The sync pulse goes high at the beginning of these columns and can, therefore, be used to clear the timing counter.

## 3-59. Clock Pulse Generator

a. The clock pulse generator produces clock pulses at the rate of 16 clock pulses per column for the data strobe generator. The clock pulses are derived from the timing gear in the card reader mechanism since the rate of rotation of the timing gear is directly proportional to that of the card drive capstans. Reluctance pickup coil A2A4PU1 in the card reader mechanism [fig. 8-9] senses the flux generated by the evenly spaced notches on the timing gear, and generates a sine wave which is filtered by capacitor A2A4C2. The sine wave period is approximately 300 $\mu \mathrm{sec}$. Eight cycles of this sine wave are generated during the time that each column of the card passes under the read photocells.
b. The reluctance pickup coil is connected across full-wave rectifier CR1 through CR4 on card A15 (fig. 823) which doubles the frequency. The resulting $6.6-\mathrm{kc}$ signal ( $150-\mu \mathrm{sec}$ period) is applied to shaper Q3, where it is amplified and converted to a pulse output with short risetimes and falltimes.


Figure 3-33. Data strobe control circuits, block diagram.

Finally, the shaped signal is amplified by inverter amplifier Z7A to produce CLK clock pulses. Since the input sine wave occurs at a rate of eight cycles per column, the output CLK clock pulses occur at 16 pulses per column.

## 3-60. Timing Counter

The timing counter is a binary counter that receives CLK clock pulses from the clock generator at the rate of 16 pulses per column and, once each column on the count of 5 , produces an output pulse near the time at which the center of the card hole is passing under the read photocells.
a. Basic Counter Operation. The binary counter consists of flip-flops Z28, Z27, Z26, and Z25 on card A14 (fig. 8-22).
(1) The basic timing input to the counter is provided by CLK clock pulses from the clock generator on PC card A15. These pulses are applied to the CL and J-inputs of flip-flop Z28. The K-input is normally at a high level supplied by AND gate Z24B.
(2) The clock input, at 16 clock pulses per column, causes $Z 28$ to change states at this rate, resulting in a square wave of eight pulses per column at the 1 output (fig. 3-36). This output is connected directly to the clock input of flip-flop Z27. On every negativegoing transition of the square wave, Z27 changes states, resulting in a square wave output of four pulses per column. This process is repeated for flip-flops Z26, Z25, and Z21. The J-input of Z26 and the K-input of Z25 are controlled by the inverted LIT signal which is high only when a card is in the read station.
(3) The four flip-flops function as a conventional binary counter as indicated ir figure 3-36 by the combination of states for the counts of 0 (0000) through 15 (1111). Since the speed at which the card passes under the card read head is approximately one
column ever 16 counts, the counter recycles once for each column.
b. Counter Synchronization. The counter is synchronized to $t$ he count of 0000 at the beginning of each column by the sync pulse from the sync generator.


Figure 3-34. Individual data strobe generation, timing diagram.


Figure 3-35. Timing counter operation.

This positive pulse, which appears at the beginning of each column oil line SNC, is pasted through OR gate Z2013 to clear flip-flops Z28, Z25, and Z21 and directly to clear flip-flops Z27 and Z26. During the time that the sync pulse appears, clocking of the first stage of the counter is disabled by AND gate Z24B, which produces a low output during the time the at the positive SNC pulse is present.
c. Card Leading Edge Control. The timing counter is preset to the count of 6 at the leading edge of the card.
(1) When no card is present at the read station, all 15 read )photocells are lighted, producing a high output signal from the all-lighted detector. This high signal disables AND gate Z2413, the low output of which prevents clock pulses front being gated into the first stage of the counter, flip-flop Z28. Simultaneously, the LIT signal is routed through OR gate Z20B to the Cinputs of flip-flop)s Z28, Z25, and Z21, and is applied directly to the S-inputs of flip-flops Z27 and Z26. The binary count is thereby preset to 0110 (6).
(2) When the leading edge of tile card reaches the read photocells, the LIT signal becomes low; enabling AND gate Z24B (since the SNC line is normally low), and counter operation is turned on. Tile time that passes between the appearance of the card leading edge at the read photocells and the appearance of tile leading edge of the first column is measured by 42 clock pulses. This is two complete 16 -count cycles of the counter plus 10 counts. Since the counter is preset to 6 , it recycles after the first 10 counts and then recycles twice again before the leading edge of the first column is reached (fig. 3-36). At that time, the count should be zero. To insure that the count is zero in case the card slipped slightly, the sync signal clears the counter to zero on the leading edge of the column as
described in b above.
d. Count of 5. The count of 5 (0101) is monitored by AND gates Z23A and Z\%23B which receive the 0 output of flip-flop Z28 and the 1 outputs of the remaining flip-flops. During the time that count of 5 is present in the counter, all inputs to the AND gates are low so that both AND gate acre enabled. The negative count-of-5 pulse at tile Z23A output is used to control the timing of the data sample ,and data < strobe pulses.
e. Data Sample Control. A data sample signal is generated from counts 5 to 8 of the timing counter to allow data to be entered into the data register at this time in each column. The data sample signal is initiated by the negative count-of-5 pulse from AND gate Z23A. This pulse is inverted by inverter Z15A to produce a positive C5 pulse which sets latch Z18. The latch remains set, until the count of 8 at. \which time counter flip-flop Z25 is set. The high C8 signal produced by Z25 at this time clears latch Z18. Thus, a high data sample (DS) signal appears at the Z18 out-put from counts 5 to 8.
f. Data Strobe Control. The data strobe lasting from count 8 to count 9 of the timing counter for each column is generated by flip-flop Z19. This flip-flop is set at count 8 by the negative transition of the DS data sample pulse and is cleared one count later by a C1A9 signal from AND gate Z22B. The C1A9 signal is high for counts 1 and 9 of the timing counter because AND gate Z22B monitors only the states of the first three flipflops with the help of AND gate Z23B. When these flipflops are ill the 001 state, Z22B is enabled. This occurs for both the counts of 1 (001) and 9 (1001).
g. Data Register Reset Control. The data register is reset at count 1 of tile timing counter for each column.

This is controlled by AND gate Z22A which, with the help of AND gate Z23B, monitors the state of the first four flip-flops. When the count is 1 (0001), AND gate Z22A is enabled to produce a high level on the register reset line (RRST). This 1 -count pulse resets the data register.

## 3-61. Sync Generator

The sync generator produces a sync pulse at the start of each column. The sync pulse is obtained by monitoring the status of all 12 Hollerith data bits that are being read by the photocells. This is accomplished by two sets of OR gates that divide the 12 data bit lines into two separate monitoring circuits, each monitoring 6 data bit lines.
a. The occurrence of a hole punched in the upper six lines (Hollerith data bits 10, 11, 12, 1, 2, or 3 ) is monitored by OR gates Z4A and Z4B. Similarly, on PC card A14 (fig. 8-22), Hollerith data bits 4, 5, 6, 7, 8, and 9 are monitored by OR gates Z8A and ZS8B. The appearance of a hole at any one of the 12 data bits results in a high level at the output, of one of the four OR gates. This, in turn, results in a high level at the output of OR gate Z7A or Z7B. The Z7A and Z7TB outputs are integrated by capacitors C 1 and C 2 to filter out transients and is then inverted to low levels by inverters Z3A and Z6B.
b. If a hole is sensed in $t$ he upper six lines of the card, the low level at the Z3A output passes through AND gate Z2B, which is enabled by the normally low level from Z3B. The low level at Z3A is also inverted by Z3B and, after integration by R3 and C3, disables AND gate Z2B after a short delay to result in a single SNCA pulse at the output of Z2B.
c. Similarly, if a hole is sensed in the lower six lines of the card, a single positive SNCB pulse is produced by AND gate Z2A.
d. The occurrence of an SNCA or SNCB pulse is monitored by OR gate Z10A which passes the pulse to flip-flop Z16G and and gate Z12B Flip-flop Z16 is initially cleared and provides a high conditioning level to AND gate Z12B. The third input to the AND gate is the NEC signal 'which is high only if the end of card photocell is covered. This must be the case if the data portion of the card is in the read station. Thus, AND gate Z12B is enabled to pass the sync pulse from OR gate Z10A to the SNC line. The negative transition at the trailing edge of the pulse immediately sets flip-flop Z16, disabling Z12B. Therefore, even if holes are sensed in both the upper and lower six lines of the card, only the first sync pulse (SNCA or SNCB) is allowed to pass through to the SNCB output line.

## 3-62. Data Register

The data register stores the 12 Hollerith bits from the photocell amplifier to insure that all data bits are available to the CCU when the data strobe is transmitted.
a. Simultaneous storage for the 12 data bits is provided by 12 latches on PC card A7 (tig. 8-15), The 12 Hollerith data bits are gated to the set inputs of the 12 latches by corresponding AND gates. For each card column, the input AND gates are conditioned at the count of 5 of the timing counter. This is controlled by the data sample signal (DS) from the timing counter. The DS signal, which is high from the count of 5 to the count of 8 , is passed through OR gates


Figure 3-36. Timing counter count sequence, timing diagram.

Z1B, Z1A, and Z2B to condition the 12 input AND gates. Therefore, at the count of 5 , the data is passed through the input AND gates, setting those latches for which a 1 data bit is received and leaving the others cleared.
b. The data remains in the register until count 1 of the timing counter at the beginning of the next column. At that time, a high level is received on register reset line RRST. This is gated through OR gate Z2A to the clear inputs of all 12 latches. A second clear input to OR gate Z2A is master reset signal RST. This insures that all latches are cleared when power is first turned on.
c. To permit a dark check of the read photocells when they are covered by the leading edge of the card, the outputs of the photocell amplifiers (which should be all low) must be gated into the data register at this time. The dark check time is defined by signal DC from the dark check portion of the alarm circuits. This signal is applied to OR gate Z1B to serve as a conditioning input for the input AND gates.

## 3-63. Offset Control

The offset control circuit drives the offset solenoid to offset header cards in the stacker. This function is controlled by the select signal from the CCU.
a. The CCU initiates offset before a header card by switching off the select (SEL) signal. The resulting negative step on select line SELA from the interface circuits on PC card A4 is inverted by inverter Z8B oil PC card A16 to set latch Z12 (fig. 8-24).
b. The Z12 latch is cleared after column 80 of the header card has passed the read photocells. This is controlled by AND gate Z4A which monitors the card and pulse (EOC) from the card and detector. At the end of column 80, the EOC signal goes high and remains high until the trailing edge of the card passes the read photocells (fig. 3-29).
c. Another condition for AND gate Z4B is that the select, (SELA) signal must be high. This prevents latch Z12 from being cleared until the SELA signal is switched on again by the CCU. Since the offset function is actuated by the step resulting from latch Z12 going from the set state to the cleared state, a second offset command to the offset solenoid cannot be generated unless the CCU switches the select signal off again to set the latch and then switches it on to allow the EOC pulse to clear the latch once more.
d. The positive OSC pulse is fed to one-shot multivibrator Q6, Q7 on PC card A15 (fig. 8-23) This results in a $140-\mathrm{ms}$ positive pulse output from the oneshot circuit which is initiated by the leading edge of the negative OSC pulse. The $140-\mathrm{ms}$ pulse is inverted by inverter Z3B to activate offset solenoid driver Q4, Q5, Q6 on PC card A1 (fig. 8-10).
c. When activated, the solenoid driver provides a ground return for -48 -volt stacker offset solenoid A3K1 (fig. 8-G). Resistor A3R1 limits the current to the solenoid. Diode A3CR1 prevents reverse overshoot when the solenoid is deenergized.

## 3-64. Alarm Circuits

## (fig. 3-37)

The alarm circuits include a series of alarm condition monitoring circuits which detect various types of alarm conditions in the card reader. Some of these alarm conditions result in an alarm stop signal sent to the CCU. Other alarm conditions result in and operator's alarm signal to the CCU. Either type of output alarm signal also causes the card feed control circuits to stop card feed. In addition, most of the separate alarm conditions result in visual indications on control panel A3. The alarm circuits also include the capability of generating an audible alarm reset signal which is sent to the CCU to reset the audible alarm.
a. Alarm Stop. An alarm stop circuit monitors the outputs of various alarm circuits for an alarm indication. When an alarm condition signal is received, the alarm stop circuit on PC card A16 (NAST) sends an alarm stop signal to the transmit interface circuits for transmission to the CCU and to the card feed control circuits on PC card A16 to stop card feed. These alarm conditions and their method of detection are described as follows:
(1) Invalid character. An invalid character ill the data bits read from the card is detected by the invalid character detector on PC card A8. The invalid detector output indication is used by the invalid character alarm circuit on PC card A14 to generate an alarm indication. This may also be generated if all read photocells are lighted at any time during the data field, as indicated by the coincidence of the LIT and data field signals.
(2) CCU sync failure. A failure of synchronism between the end of block and end of message signals received from the CCU with the data strobe pulses generated by the card reader are detected by the CCU sync check circuit on PC card A15. The CCU sync failure signal causes the alarm stop circuits to activate an out-of-sync visual indication on control panel A3. To prevent a sync check failure signal unless the card reader is operating with the CCU, a gated select signal from the card feed control disables the CCU sync check failure indication unless a select signal is being received front the CCU.
(3) Light check failure. A failure of all read photocells that should be lighted when no card is present in the read station is detected by their light check circuit on PC card A14 which monitors the beginning-of-card and end-of-card photocell signals
to determine card position and also monitors the LIT signal to determine when the read photocells are lighted. A light check failure results in a photocell check failure signal, which activates a visual indicator on control panel A3 besides activating the alarm stop signal.
(4) Dark check failure. A failure of all read photocells that should be darkened when the leading edge of the card is passing over the read photocells, is detected by the dark check circuit on PC card A14. To insure that this check in made at the proper time, the dark check circuit monitors the beginning-of-card photocell signal and a count output of the timing counter in the data strobe control circuit. Either a light check or dark check failure is indicated by a photocell failure signal, which activates a visual indicator on control panel A3 besides activating the alarm stop signal.
(5) Pick failure. A failure of a card to reach the read station within approximately 115 ms of a pick command is detected by the pick failure alarm circuit on PC card A15. This circuit operates by monitoring the duration of the advance solenoid signal from the card feed control circuits, since this signal lasts until a card reaches the read station. A pick failure activates an operator's alarm. A sync failure is generated if a card passes through the read station after a pick failure is declared.
(6) Card jam. A card jammed in the read station is detected by the card jam circuit on PC card A15. The presence of a card in the read station is detected by a read time circuit on PC card A14. This circuit produces a read time signal when the all-lighted detector indicates that one or more or the read photocells is covered. The card jam circuit performs its function by checking that the read time signal does not last more than approximately 400 ms .
(7) Cancel. When the CCU indicates that a data block is to be canceled by sending a cancel signal to the card reader, the cancel signal is monitored by a cancel control circuit in PC card A15. If the card reader is also receiving a select signal from the CCU, the correct control circuit produces a cancel control signal which activates the alarm stop circuits and a visual indicator on the control panel.
b. Operator's Alarm. An operator's alarm signal is generated by the operator's alarm circuit when any one of three alarm conditions occurs. The operator's alarm signal is sent through the transmit interface circuit to the CCU and is also sent to the card feed control circuits to stop card feed. The alarm conditions are detected as follows:
(1) Hopper empty. A hopper empty condition is detected by a card alarm circuit on PC card A15. This circuit produces a card alarm signal if the hopper empty photocell is illuminated after the last
card has left the read station and EDM has not been received from the CCU. The absence of a card in the read station is indicated by the inactive state of the cycle signal from the card feed control circuits. The card alarm signal activates a visual indicator on control panel besides activating the operator's alarm circuit.
(2) Stacker full. A stacker full condition is detected by a sensing switch at the stacker. This switch is monitored by the card alarm circuit and causes generation of a card alarm signal.
(3) Pick failure. A pick failure condition detected by the pick failure alarm circuits results in a pick failure signal which activates the operator's alarm circuit.
c. Audible Reset. When the AUDIBLE RESET alarm pushbutton on the control panel is pressed, a corresponding control circuit on PC card A16 activates an audible alarm reset signal which is routed through transmit interface circuits to reset the audible alarm in the CCU; however, this signal is disabled unless the CCU operator has assigned the card reader to the CCU by pressing a pushbutton on the CCU. If not, the absence of an assigned signal from the receiver interface circuits inhibits the audible alarm reset control.

## 3-65. Invalid Character Detector, Principles

a. The invalid character detector monitors the 12 Hollerith data bits read from the card and checks them for invalid combinations. An analysis of the Hollerith characters listed in table 3-3 shows that there are five groups of invalid combinations-
(1) Two or more punches in bits 1 through 7, 9.
(2) Punches in bits 10 and 11 plus one or more punches in bits 1 through 7, 9 .
(3) Punches in bits 10 and 12 plus one or more punches in bits 1 through 7, 9 .
(4) Punches in any of the following bit combinations:
(a) 11 and 12 .
(b) 8 and 1 .
(c) 8 and 9 .
(d) 8 and 2 and 11 .
(e) 8 and 2 and 12 .
(f) 8 and 10 and 11.
(g) 8 and 10 and 12 .
(5) Punches for the 14 characters encircled in table 3-3 that were made invalid by backplane wiring.
b. The invalid character detection requirements for the first three groups of invalid combinations (a(1), (2), and (3), above) can be represented by the array shown in table 3-4. This array shows the intersection of three rows and three columns of numbers

## Change 1 3-43



Figure 3-37. Alarm circuits, block diagram.
representing Hollerith bits. The first column represents Hollerith bits 1, 4, and 7. The third position in the third column represents a special combination of bits: 10 and either 11 or 12 , that is, $10(11+12)$.
c. The array of table 3-4 demonstrates the first three groups of invalid combinations if the statement is made that a combination of card bits represented by any two positions in the array are invalid. The first invalid combination group (a(1) above) involves bits 1 through 7 and bit, 9 , all of which occupy separate positions in the array. If any two of these bits are punched, an invalid combination exists. The second and third invalid combination groups (a(2) and (3), above) involve the 10 $(11+12)$ combination since neither of the two possibilities in this combination (10 and 11 or 10 and 12) is permitted to coexist with the bits in the other eight positions ( 1 through 7,9 ) according to the rules of the second and third groups.

Table 3-4. Invalid Character Detection Array

|  | Columns |  |  |
| :---: | :---: | :---: | :---: |
|  | 1 | 2 | 3 |
|  | 4 | 5 | 6 |
|  | 7 | 9 | $10(11+12)$ |

d. The requirement that no two positions in the array of table 3-4 are permitted to coexist can be implemented by determining which column and which row of the array contain a punched bit. If bit 6 is punched, the second row and the third column are activated. Similarly, if any of the nine array positions are punched, only one column and one row are activated; this is a permissible combination. However, if any two positions in the array are punched, two columns or two rows are activated. For example, if bits 3 and 6 are punched simultaneously, rows 1 and 2 as well as column 3 are activated; this is an invalid combination.

## 3-66. Invalid Character Detector Operation

a. The signals representing the nine positions of the array of table 3-4 are Hollerith data bits 1 through 7 and 9 , and Hollerith combination 10 (11+12). The Hollerith data bits are supplied from the register on PC card A7. The $10(11+12)$ combination is developed in the Hollerith-to-octal converter on PC card A8 para 351).
b. To determine which rows and columns of the array are activated at any time, the signals representing the nine positions of the array are fed to six OR gates on PC card A8 (Z7A, Z11B, Z15B, Z7B, Z11A, and Z15A) representing the three rows and three columns (fig. 816). The equations for the six OR gate outputs are as follows:
(1) Column $(Z 7 A)=1+4+7$.
(2) Column $2(\mathrm{Z} 11 \mathrm{~B})=2+5+9$.
(3) Column 3 (Z15B) $=3+6+10(11+12)$.
(4) Row 1 (Z7B) $=1+2+3$.
(5) Row $2(\mathrm{Z} 11 \mathrm{~A})=4+5+6$.
(6) Row 3 (Z15A) $=7+9+10(11+12)$.
c. To implement the rule that no two rows or two columns can be activated simultaneously the three column signals are fed to AND gates Z8A, Z8B, and Z12A in three possible combinations of two simultaneous columns. If any one of these three AND gates is enabled, an invalid condition is indicated. This is monitored by OR gate Z20A which produces a high output if any one of the three AND gates is enabled. Similarly, the three row signals are fed to AND gates Z12B, Z16A, and Z16B in the three possible combinations of two simultaneous rows. The three AND gate outputs are monitored by OR gate Z20B which produces a high output if any one of the three AND gates is enabled.
d. The outputs of OR gates Z20A and Z20B are fed to expander inputs to OR gate Z3B so that either a double row or double column combination results in a low invalid output from Z3B. This is sent to the invalid character alarm circuit on PC card A14 for timing control.
e. The special invalid character combinations listed in paragraph 3-65a(4) are monitored by OR gate Z23A. When any one of these combinations exists, Z23A produces a high output which causes Z31B to produce a low invalid output.
$f$. The invalid condition of punches in both bits 11 and 12 is monitored by AND gate Z18A which controls one of the inputs to OR gate Z23A. The other two inputs to Z23A are controlled by AND gates Z19A and Z19B. A common input to both AND gates is Hollerith bit 8 since all of the remaining special invalid combinations in paragraph 3-65a(4) ,are marked by the presence of this bit. OR gate Z23B, which controls the other input to Z19B, monitors Hollerith bits 1 and 9 . If either of these bits is punched, Z23B produces a high output which enables Z 19 B if bit 8 is punched.
g. The other two inputs to AND gate Z19A are controlled by OR gate Z14B which monitors bits 2 and 10, and OR gate Z17B which monitors bits 11 and 12. If bit 8 is punched at the same time as either bit 12 or 10 and either bit 11 or 12, an invalid combination
is indicated. Thus, AND gate Z19A is then enabled and a high output is routed through OR gate Z23A to OR Z3B to cause a low output on the INVALID line.
$h$. The 14 circled characters in table 3-1 are detected by routing the corresponding decode matrix output lines to OR gates Z1A, Z1B, Z2A, Z2B, and Z3B on PC card A1 (fig. 8-10). When any one of these 14 characters is decoded, a high level is produced on inhibit line XINH. If the character is wired for inhibit this high level is routed directly to OR gate Z3B an PC card A8 to cause a low level on the INVALID line.

## 3-67. Invalid Character Alarm Circuit

The invalid character alarm circuit produces an invalid character alarm signal when an invalid character is detected by the invalid character detector or if all photocells are lighted at any time during the data field (columns 1 through 80).
a. If the invalid character detector senses an invalid character, a low level invalid signal (INV) is applied to AND gate Z17B on PC card A14 (fig. 8-22). This AND gate is also controlled by the data field signal from OR gate Z20A in the data field detector since an invalid character is an alarm condition only if it occurs during the data field when the data field line is low. If both the INVALID and data field lines are low, the not function of the data strobe is gated through Z17B to set latch Z1. The resultant high invalid character alarm signal (INC) appears at the 1 output of the latch.
b. Latch Z1 can also be set under control of AND gate Z17A when the read photocells are all lighted during the data field. This condition is identified by low signals on the inverted LIT line from the all lighted detector and on the not data field line from the data field detector.

## 3-68. CCU Sync Check Circuit

The CCU sync check circuit generates a sync failure signal unless an end of block signal is received from the CCU in the time period between the trailing edge of the 80th data strobe and the leading edge of the end-of-card signal.
a. The end of block (EOB) signal from the receive interface circuits on PC card A4 is routed to AND gate Z1B on PC card A15. The AND gate is conditioned by a high select A (SELA) signal when the card reader is selected by the CCU. The gated EOB signal clears latch Z15. The set side of this latch is controlled by the data strobe (DST) signal from the data strobe control circuits on PC card A14. As the card passes through the read station, the data strobe pulses keep latch Z15 in a set state. If an FOB pulse occurs following the 80th data strobe, the latch remains in the clear state until the first data strobe
of the next card. However, if the EOB pulse does not occur or occurs before the 80th data strobe, flip-flop Z15 is not cleared and remains in the set state. ' This indicates a CCU sync check failure.
b. To keep latch Z15 cleared between messages, the in message/out of message state of the card reader is monitored by latch Z 5 . This latch is set to the in message state by the first gated step (GS) signal> from PC card A16. The in message state lasts until one of four out of message conditions occurs. One of these is a cancel condition detected by AND gate Z2A in the cancel control circuit (bara 3-69). Another is deassignment by the CCU operator, which is indicated by a high level on not assigned line NASG from the receive interface circuits. The NASG signal is routed through OR gate Z9A to latch Z5. The detection of a normal end of message by the CCU results in a high level on end of message line EOM. If the card reader is selected, the high level on select line SELA is combined with the high level on line EOM to enable AND gate Z1A. The resulting high output is routed through OR gate Z9A to latch Z5. The final condition clearing latch Z5 is a high level on master reset line RST.
c. When latch $\mathrm{Z5}$ is set in the out of message state, the Z5A output is a high level which keeps latch Z15 cleared, preventing a CCU sync failure indication. Alternately when the latch is cleared, a high level at the Z5B output enables detection of a hopper empty condition by the card alarm circuit.

## 3-69. Cancel Control Circuit

a. When a cancel signal is received from the CCU during a data block, the cancel control circuit initiates an alarm stop and causes CANCEL indicator DS2 on the control panel to be lighted.
b. The cancel signal is detected by AND gate Z2A on PC card A15 (fig. 8-23). If the cancel signal is received from the CCU during a data block when the select line is active, the receive interface circuits supply low levels on line NCAN and NSEL. These low levels enable AND gate Z2A which sets latch Z6. The resulting high output of the latch on the DCAN line activates a lamp driver on PC card A3 to energize CANCEL indicator DS2 on the control panel. The DCAN signal is also fed to the alarm stop circuit to cause an alarm stop signal.

## 3-70. Light Check Circuit

a. The light check circuit performs a light check before the time when the leading edge of the card reaches the end of card photocell position A, figure 330 , and after the time when the trailing edge $o$ ! the card leaves the beginning of card photocell (position F). The light check is a check that all of the 12 reading photocells are illuminated at this time.
b. The light check is performed by AND gate Z14A on card A14 fig. 8-22). The timing of tile light check is controlled by the not beginning of card (BCN) and not-end-of card (NEC) signal inputs to AND gate Z14A. Both signals are derived from the photocell amplifier circuit. on PC card $A 6$ with the $B C N$ signal received directly and the ECN signal developed by inverter Z15 from end-of-card input EC. Since BCN and NEC signals are complements of those shown in figure 3-30, they are both flow only when both the beginning and end-of-card photocells are illuminated. If any of the reading photocells are not illuminated at any time before position A and after position F, the LIT signal, monitored by AND gate Z14A from the all-lighted detector on PC card A6, is also low. The resulting high output of Z14A sets latch $\mathrm{Z9}$ to indicate the light check failure condition. Latch Z9 may also be set as a result of a dark check failure.

## 3-71. Dark Check Circuit

The dark check circuit performs a dark check during the time when the leading edge of the card passes over the read photocells. The dark check consists of determining that none of the read photocells are activated at this time. Since the top corner of the leading edge is crosscut, it is necessary to insure that, the dark check is not performed until the crosscut portion is passed; otherwise, light getting through the crosscut region might actuate one of the photocells, thereby giving a false error indication.
a. To insure that the dark check does not take place until after the crosscut region, the dark check is performed 31 counts of the data strobe generator after the leading edge of the card has passed. Thus, referring to figure 3-35, the dark check is performed on the second count of 5 after the leading edge.
$b$. The timing of the dark check is controlled by AND gate Z13B on PC card A14 (ig. 8-22). When enabled, this gate passes a negative count-of-5 pulse from AND gate Z23A in the data strobe timing counter. One gating condition for this AND gate is a low level on the not beginning-of-card (BCN) photocell amplifier line. As indicated in figure 3-35, this occurs up to the time when the first column appears under the read photocells. Thus, the dark check can only occur during the time when the leading edge of the ,card is under the read photocells.
c. The other gating condition for AND gate Z13B is the 1 output of flip-flop Z21. This flip-flop functions as a fifth stage of the data strobe timing counter, being initially cleared at. the start of operation, and then being set for the first time on the count of 16 when the fourth flip-flop stage Z25 is cleared. This is controlled by the negative-going 1 output of Z25 connected to the toggle input to Z21. The flip-flop
remains set until 16 counts later, when Z 25 is again cleared.
d. As shown in figure 3-38 count operation of the data strobe timing counter begins on the count of 6 at the leading edge of the card. Thus, the first count of 5 does not occur until after Z21 is set on the count of 16. At that time, the high level at the 1 output of the flip-flop disables AND gate Z13B. Alien the next count of 5 occurs 16 counts later, Z21 is in the cleared state and a low level is provided for Z13B. AND gate Z13B is enabled by the count of 5 pulse to produce a positive dark check (DC) pulse. This is inverted by inverter Z13A to produce a negative dark check enable (DCE) pulse.
e. The positive DC pulse is routed to the data register to permit storage of the information sensed by the read photocells at this time.
$f$. The negative DCE pulse is sent to AND gate Z8B on PC card A13 (fig. 8-21) to allow this gate to sample the state of AND gate Z12A. The purpose of AND gate Z12A is to check for the presence of a decoded space character 00100000 (least, significant bits on right) at, the ASCII output. This character is produced whenever all 12 read photocells are covered. To check for this character, the true-functions of all eight, ASCII bits except bit 6 (ASCII BIT 32) are monitored by AND gate Z12A. The not-function of bit 6 is supplied by OR gate Z8A which functions as an inverter. Thus, whenever a space character is present, at the ASCII output,, Z12A is enabled and supplies a high level to disable AND gate Z8B.
g. If a space character is not, detected at, the time of the dark check, the output of Z12A is low and the negative DCE pulse momentary enables AND gate Z8B to result in a positive pulse on the dark check fail line (DCF). This is returned to PC card A14 to set latch Z9. Since Z9 is set by either a light, check or dark check failure, its resulting high output is identified as a photocell check failure (PHCK).

## 3-72. Pick Failure Alarm Circuit

a. The pick failure alarm circuit, monitors the pick command to the picker solenoid driver and generates an alarm indication if the picked card fails to reach the end-of-card photocell at the beginning of the read station will approximately 115 ms of the step command which initiated the pick command. This function is performed by monitoring the width of the pick solenoid drive pulse since this pulse is terminated by the darkening of the end-of-card photocell. If the pulse width is longer than 115 ms , a failure is indicated.
b. The advance solenoid drive pulse (ASD) from the card feed control circuit on PC card A16 is fed to time delay circuit, Q1, Q2 on PC card A15 (fig. 8-23). If the AI)V pulse lasts longer than 115 ms , the


Figure 3-38. Dark check circuit, timing diagram.
time delay produces an output pulse at the end of the $115-\mathrm{ms}$ interval which sets latch Z14. This results in a high DPKF pick failure signal at the 1 output of the latch. If the ADV pulse lasts less than 115 ms , no output pulse is produced by the time delay circuit and the DPKF line remains low. \l'hen activated, the DPKF line energizes a lamp driver on PC card A3 to light PICK FAIL indicator DS8 on the control panel. By causing an operator alarm, the DPKF line also causes the picker solenoid to be deenergized.

## 3-73. Card Alarm Circuit

The card alarm circuit produces an alarm indication on either a hopper empty or stacker full condition.
a. When the card render is assigned to the CCU, the hopper empty condition is considered an alarm condition only after the CCU sends a step/data acknowledge signal requesting a new card to be picked. This results in an in-message signal to AND gate Z11A on PC card A15 [fig. 8-23. The other input to Z11A is controlled by AND gate Z7B which produces a high output if the hopper empty photocell is illuminated following completion of a card cycle. Thus, AND gate 27B is enabled by a low level on the HPN line from the photocell amplifiers and a low level on the CYCL line from the card feed stop control circuits.
b. The high output of AND gate Z11A sets latch Z13, resulting in a high level on card alarm line CA. This signal is gated through OR gate Z4A to the DCA line which activates a lamp driver on PC card A3, energizing CARD ALARM indicator DS7 on the control panel. The CA signal is also gated through OR gate Z16B to result in an operator's alarm signal to the CCU.
c. If the card render is not assigned to the CCU. the hopper empty card is not condition is not dependent. on the receipt of a step/data acknowledge signal from the CCU. In this case, the high level on the HPE output of AND gate Z7B enables AND gate Z11B which is conditioned by a high level on not assigned line NASG. The resulting high output
feed. The alarm stop signal is generated as a low level on line NAST when any one of a number of alarm stop conditions occurs.
a. The NAST signal is produced by OR gate Z16A on PC card A15 (fig. 8-23), This OR gate is activated by a high level on the DCAN line from latch Z6 whenever a data block is canceled by the CCU. Three other alarm stop conditions are monitored by OR gate Z4B which supplies a second input to OR gate Z16A. Thus, when an invalid character (INC), photocell check failure (PHCK), or card jam (DCJ) occurs, the corresponding line goes high, activating OR gate Z4B and, in turn, Z16A.
b. The third input to OR gate Z16A is controlled by latch Z 12 which is set whenever the card reader is assigned to the CCU but is out of sync. Thus, OR gate Z9B is activated by latch Z15 in case of a CCU sync check failure and is activated by pick failure line DPKF in case of a card pick failure. In either case, the high output of Z9B enables AND gate Z10A after the card being processed has left the read station (cycle complete line CC is high) as long as an alarm stop has not yet been generated (line NAST is high). The high output, of Z10A sets latch Z12 to activate OR gate Z16A and places a low level on line NAST.
c. The high output of latch Z 12 is also routed on line DSYN to a lamp driver PC card A3 which energizes OUT of SYN indicator DS6 on the control panel. The indicator remains lit until latch Z 12 is cleared. This occurs either on an alarm reset condition (alarm reset, line ARST goes high) or when the card reader is deassigned from the CCU (not assigned line NASG goes low).

## 3-77. Operator's Alarm Circuit

The operator's alarm circuit consists of OR gate Z16B on PC card A15 (fig. 8-23) This gate, produces a low level operator's alarm signal on line NOA for transmission; to the CCU by the transmit interface circuits if either a card alarm or pick failure occurs. Thus, if either card alarm signal CA or pick failure signal DPKF goes high, the OR gate is activated and places low level on the NOA line. The NOA signal is also routed to the card feed stop control circuit to stop automatic card feed.

## 3-78. Audible Alarm Reset Control Circuit

If the card reader is assigned by the CCU, the audible alarm reset control circuit generates an audible alarm reset signal (AAR) when AUDIBLE RESET switch Z1 on the control panel is pressed. This signal is fed through the transmit interface circuits to the CCU to reset the audible alarm.
a. Closure of the AUDIBLE RESET switch Z1 contacts transfers a high level to line ARO which is fed to debouncing latch Z5 on PC card A16 (fig. 8-24) The resulting positive step at the Z5B output of the latch is
converted into a sharp positive pulse by differentiator C1, R9. The pulse is then coupled through OR gate Z17A which activates line AAR. Positive feedback through capacitor C2 makes the OR gate function as a single shot. The pulse width is determined by the time required to charge up C1 through resistor R10 to a potential at which the feedback voltage is insufficient to keep Z17A activated. At that time, the Z17A output returns to a low level and C2 quickly discharges through diode CR1.
b. To prevent generation of the AAR pulse when the card reader is not assigned by the CCU, a low level on assigned line ASG from the receive interface circuits is inverted to a high level by inverter Z10A. This prevents $Z 5$ from initiating a step when the switch $Z 1$ is pressed.

## 3-79. Alarm Reset Control Circuit

An alarm reset signal is generated for the a] arm stop circuits when any of the three card feed switch indicators on the control panel (SINGLE FEED Z4, LOCAL TEST Z5, and START Z7) is pressed, or when RESET switch S1 (on logic assembly front panel) is pressed, and when power is turned on to the card reader. However, the alarm reset signal is disabled during a block in which a cancel signal is being received from the CCU.
a. A power-on reset or a pushbutton reset activates OR gates Z20B in the card feed stop control circuit para 3-47). The resulting high level activates OR gate Z15B which places a low level on not alarm reset line NAR. The NAR line is also activated when any one of the three card feed switch-indicators is pressed. In that case, OR gate Z15B receives a positive start pulse from AND gate Z26A in the card feed control circuit.
b. The NAR line is fed to AND gate Z2B on PC card A15 fig. 8-23 which becomes enabled if AND gate Z2A supplies a conditioning low level. The resulting high level on alarm reset line ARST clears the various alarm stop flip-flops.
c. The alarm reset function is disabled by AND gate Z2A if the CCU supplies a cancel signal while the card reader is selected. The resulting low levels on the NCAN and NSEL lines from the receive interface circuits enable AND gate Z2A, disabling AND gate Z2B, and preventing the ARST signal from going high.

## 3-80. Transmit Interface Circuits

The ready signal from the ready control circuit is shifted from card reader switching levels ( 0 volt and +4.5 volts) to CCU interface switching levels (open circuit and 0 volt) by the transmit interface circuits. (open circuit and 0 volt) by the transmit interface circuits. This permits the CCU to send the select signal through the receive interface circuits. This permits the CCU to send the select signal through the receive interface circuits. When the select signal is present, the eight output ASCH data bits and the data strobe are gated through the transmit interface circuits to the CCU.
a. Ready Signal. The ready signal from the ready control circuit on PC card A16 is inverted to an active level of 0 volt and an inactive level (open circuit by transmitter (A) on PC card A4 (fig. 8-12), The resulting transmit ready (TRDY) output is sent to the CCU.
b. Data Strobe. The data strobe (DST) from the data strobe control circuits on card A14 is gated into transmitter (J) on PC card A5 by the SEL B select line from the receive interface circuits (fig. 8-13). When the select input from the CCU is active, the SEL B line is high and the positive DST strobe pulses are accepted and inverted to produce negative pulses (TDST) to the CCU switching from +6.2 volts to -6.2 volts.
c. ASCII Outputs. The eight output ASCII data bits (DB1 through DB8) from the Hollerith to ASCII encoder are gated into transmitters (A) through (H) on PC card A5 by the select line from the receive interface circuits. The SEL A select input is buffered by OR gates Z1A and Z1B to condition the eight transmitters. When the CCU has selected the card reader, a high level on each input bit line results in a +6.2 -volt output. A low level on each input line results in a-6.2-volt output.
d. Alarm Stop and Operator Alarm Signal. The not alarm stop (NAST) and not operator alarm (NOA) signals from the alarm logic control circuits on card A15 are inverted to an active level (open ckt) and an inactive level of 0 volt by transmitters (B) and (C), respectively, on PC card A4 (fig. 8-12). The resulting transmit TAST and TOA outputs are open ckt when an alarm condition exists and at 0 volt when no alarm condition exists.
e. Audible Alarm Reset Signal. The audible alarm reset signal (AAR) from the alarm control circuits is fed to transmitter (D) on PC card A4. When the card reader is assigned to the CCU, the ASGD line from the receive interface circuits goes high. This conditions transmitter (D) to produce 0 volt on line TAAR to the CCU, resetting the audible alarm in the CCU. If either input goes low, the TAAR output is an open circuit.

## 3-81. Detailed Operation of Discrete Circuits on PC Card A1 <br> fig. 8-10

a. Power On Reset Circuit. The power on reset circuit produces a power on reset pulse when power is turned on. Power turn-on results in the +4.5 -volt dc supply level being coupled through resistor R3 to the circuit output. However, the -48 -volt supply current gradually charges up capacitors C 1 and C9 through resistor R2. The voltage at the junction of C1, C9, and R2 is applied to 16 -volt Zener diode VR1 to the output.

When sufficient charge is built up in C1 and C9 to drive VR1 into conduction, the output begins dropping from the +4.5 -volt level established through resistor R3. Thus, at the moment when conduction begins, the voltage at the junction of $\mathrm{C} 1, \mathrm{C} 9$, and R 2 is approximately -11.5 volts. As charge continues to build up, the output voltage continues to drop until it reaches 0 volt. The output is prevented from going below this value by diode CR1.
b. Solenoid Drivers. Solenoid driver Q1, Q2, Q3 is activated by a 0 -volt input to resistor R5. This results in a negative voltage at the junction of voltage divider R5, R6 to drive transistor Q1 into conduction. Conduction of Q1 causes a 0 -volt level at the Q1 collector which supplies current to the base of Q2. This allows transistor Q2 to go into conduction so that a -12 -volt level is coupled through resistor R10 to drive transistor Q3 into conduction. The Q3 collector is connected through the external solenoid winding to the -48 -volt supply. Thus, the solenoid draws current from the -48volt return line (ground) through Q3. If the input to the solenoid driver goes to +4.5 volts, all operations are reversed and Q3 is cut off so that the solenoid is deenergized. Capacitor C2 slows down the rise and fall times of the Q3 output, and diode CR3 sets the bias for the base of Q3 at +0.7 volt when Q2 is cut off. Solenoid driver Q4, Q5, Q6 operates in a similar manner.

## 3-82. Detailed Operation of Discrete Circuit Logic Elements

The detailed circuit operation of discrete circuit logic elements is described ih paragraphs 3-83 through 3-86. The component makeup of each type of logic element is shown in figures 3-39 hrough 3-45. However, since one example of each type is shown in these figures, refer to table 3-5 for a detailed listing of the corresponding components in the logic element of each type.

## 3-83. Detailed Operation of Discrete Circuit Logic Elements on PC Card A4

a. Type RCVR-1A Interface Receiver (fig. 3-39). The type RCVR-1A receiver converts a 0 -volt input from the CCU to +4.5 volts and an open circuit input from the CCU to 0 volt. When the transmitting source comes an open circuit, the input signal becomes +6.2 volts due to the reference voltage established by Zener diode VR4. This voltage is coupled to the base of transistor Q8 driving Q8 into conduction. This result in a 0 -volt output at the Q8 collector. When the input signal goes to

| PC card |  | Logic element referenc |  |  |  |  |  |  |  | Component reference designation |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A4 | XMTR-1A | (A) | R1 | R2 | R3 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Q1 |  | (B) | R4 | R5 | R6 | Q2 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (C) | R7 | R8 | R9 | Q3 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | XM-TR-1B | (D) | R10 | R11 | R12 | CR | CR2 | Q4 |  |  |  |  |  |  |  |  |  |  |  |
|  | RCVR-1B | (E) | R13 | R14 | R15 | R16 | CR3 | Q5 | VR1 |  |  |  |  |  |  |  |  |  |  |
|  |  | (F) | R17 | R18 | R19 | R20 | CR4 | Q6 | VR1 |  |  |  |  |  |  |  |  |  |  |
|  |  | (F) | R17 | R18 | R19 | R20 | CR4 | Q6 | VR1 |  |  |  |  |  |  |  |  |  |  |
|  |  | (G) | R21 | R22 | R23 | R24 | CR5 | Q7 | VR3 |  |  |  |  |  |  |  |  |  |  |
|  | RCNVR-1A (H) |  | R25 | R26 | R27 | R28 | Q8 | VR4 |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (J) | R29 | R30 | R31 | R32 | Q9 | VR5 |  |  |  |  |  |  |  |  |  |  |  |
|  | RCVR-1C | (K) | R33 | R34 | R35 | R36 | R37 | R38 | R39 | R40 | R41 | CR6 | Q10 | Q11 | Q12 |  |  |  |  |
| A5 | XMTR-2 | (A) | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 | R9 | R10 | C1 | Q1 | Q2 | Q3 | Q4 | CR1 | CR2 |
|  |  | (B) | R11 | R12 | R13 | R14 | R15 | R16 | R17 | R18 | R19 | R20 | C2 | Q5 | Q6 | Q7 | Q8 | CR3 | CR4 |
|  |  | (C) | R21 | R22 | R23 | R24 | R25 | R26 | R27 | R28 | R29 | R30 | C3 | Q9 | Q10 | Q11 | Q12 | CR5 | CR6 |
|  |  | (D) | R31 | R32 | R33 | R34 | R35 | R36 | R37 | R38 | R39 | R40 | C4 | Q13 | Q14 | Q15 | Q16 | Q17 | CR8 |
|  |  | (E) | R41 | R42 | R43 | R44 | R45 | R46 | R47 | R48 | R49 | R50 | C5 | Q17 | Q18 | Q19 | Q20 | CR9 | CR10 |
|  |  | (F) | R51 | R52 | R53 | R54 | R55 | R56 | R57 | R58 | R59 | R60 | C6 | Q21 | Q22 | Q23 | Q24 | CR11 | CR12 |
|  |  | (G) | R61 | R62 | R63 | R64 | R65 | R66 | R67 | R68 | R69 | R70 | C7 | Q25 | Q26 | Q27 | Q28 | CR13 | CR14 |
|  | XMITR-2 | (H) | R71 | R72 | R73 | R74 | R75 | R76 | R77 | R78 | R79 | R80 | C8 | C29 | C30 | Q31 | Q32 | CR15 | CR16 |
|  |  | (J) | R81 | R82 | R83 | R84 | R85 | R86 | R87 | R88 | R89 | R90 | C9 | Q32 | Q33 | Q34 | Q35 | CR17 | CR17 |
| A6 | PHOTO | (A) | R1 | R2 | CR1 | Q1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | AMPL | (B) | R3 | R4 | CR2 | Q2 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (C) | R5 | R6 | CR3 | Q3 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (D) | R7 | R8 | CR4 | Q4 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (E) | R9 | R10 | CR5 | Q5 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (F) | R11 | R12 | CR6 | Q6 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (G) | R13 | R14 | CR7 | Q7 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (H) | R15 | R16 | CR8 | Q8 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (J) | R17 | R18 | CR9 | Q9 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (K) | R19 | R20 | CR10 | Q10 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (L) | R21 | R22 | CR11 | Q11 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (M) | R23 | R24 | CR12 | Q12 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (N) | R25 | R26 | CR13 | Q13 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (P) | R27 | R28 | CR14 | Q14 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | (Q) | R29 | R30 | CR15 | Q15 |  |  |  |  |  |  |  |  |  |  |  |  |  |

0 volt, transistor Q8, is cut off and a +4.5 -volt output is coupled through resistor R28 to the load.
b. Type RCVR-1B Interface Receiver (fig. 3-40). The type RCVR-1B receiver operates in tile same way as the RCVR-1A receiver described in a above, except coupling is accomplished by constant voltage drop diode CR3 and resistor R13.
c. Type RCVR-1C Interface Receiver (fig. 3-41). The type RCVR-1C interface receiver converts a +6.2volt input, from the CCU to +4.5 volts and a -6.2 -volt input to 0 volt. A +6.2 -input causes transistor Q10 of difference amplifier Q10, Q11 to go into conduction and causes transistor Q11 to go into cutoff. The negative voltage at tile collector of Q10 is coupled through resistor R38 to drive transistor Q12 into cutoff. Thus. the output assumes the +4.5 -volt level supplied through resistor R41. If, however the input to the circuit is -6.2 volts, the base of Q10 assumes a negative potential established through resistors R33 and R34, and Q10 is driven into cutoff and Q11 into conduction. The positive level at the collector of Q10 drives Q12 into conduction so that the output goes to 0 volt..
d. Type XMTR-1A Interface transmitter (fig. 3-42). Inputs from the card reader logic circuits switching between 0 volt and +4.5 volts are coupled through biasing network R1, R2, and R3 to the base of inverter Q1. When the input is 0 volt, Q1 is cut off and supplies an open circuit to the CCU. which provides a connection through a load resistor to +6.2 volts. When the input is +4.5 volts, Q1 is driven into conduction, resulting in a 0 -volt output to the CCU.
e. Type XMTR-1B Interface Transmitter(fig. 3-43). The type XMTR-1B transmitter operates in the sample way as the XMTR-1A transmitter described in $d$ above, except diodes CR1 and CR2 are added to provide and function for two input signals, both of which must be


Figure 3-39. Type RCVR-1A interface receiver, schematic diagram.
+4.5 volts to produce the 0 -volt output.

## 3-84. Detailed Operation of Discrete Circuit Logic Elements on PC Card A5

a. The type XMTR-2 interface transmitter on PC card A5 fig. 3-44) receives card reader inputs switching between 0 volt and +4.5 volts dc at AND gate diodes CR1 and CR2. When both inputs are +4.5 volts, the diodes are cut off and bias network R1, R2, R3 drives transistor Q1 into conduction. Loading for Q1 is provided by resistors R4 and R5. The drop in voltage at the junction of R4 and R5 turns on transistor Q2 to result in a +12 -volt level at the Q2 collector. This drives transistor Q3 into conduction and transistor Q4 into cutoff. Thus, the -6.2 volt supply voltage is drawn through Q3 and resistor R8 to the circuit output.
b. When a 0 -volt level is applied to either input diode CR1 or CR2, bias network R1, R2, and R3 allows Q1 to go into cutoff. The resulting positive +12 voltoutput of Q1 cuts off Q2 so that a negative voltage appears at the Q2 collector. This voltage drives Q4 into conduction and Q3 into cutoff. Thus, the -6.2-ivolt supply is drawn through Q4 and resistor R9 to the circuit output.

## 3-85. Detailed Operation of Discrete Circuit Logic Elements on PC Card A6

The type PHOTO AMPL photocell amplifier on PC card A6 (fig. 3-45) is controlled by the output of a photocell connected to a +4.5 -supplly. When the photocell is dark, it acts as an open circuit. Thus, transistor Q1 is biased on by -12 volts through resistor R1. Diode CR1 in the emitter circuit of Q1 provides a constant voltage drop, and the output voltage across load resistor R2 is approximately 4.0 volts. When the photocell is lighted, the current flowing through the photocell builds up a 16volt drop


Figure 3-40. Type RCVR-1B interface receiver, schematic diagram.


Figure 3-41. Type RCVR-1C interface receiver, schematic diagram.
across resistor R1 so that a +4.0 - volt level at the base of Q1 drives into cutoff. This results in a 0 -volt output at the Q2 collector.

## 3-86. Detailed Operation of Discrete Circuits on PC

 Card A15(fig. 8-23)
a. Time Delay Q1, Q2, Initially, with a +4.5 -volt input applied across bias resistors R2 and R3, transistor Q1 is conducting and timing capacitor C 1 is-discharged. Unijunction transistor Q2 is not conducting. The time delay is triggered by a negative input pulse switching from +4.5 volts to 0 volt, which is applied across R2 and R. 3 to cutoff transistor Q1. This allows


Figure 3-42. Type XMTR-1A interface transmitter schematic diagram.

C 1 to charge through charging resistor R4. If the input pulse is still low after 115 ms , the voltage across C1 becomes sufficiently high to fire Q2. This results in a +4.5 -volt output established by resistors R5 and R6. Once Q2 is fired, the current drawn from capacitor C1 to the Q2 emitter discharges C1 quickly until not enough current is as available to maintain conduction through Q2. Thus, Q2 is cutoff and the output pulse is terminated.
b. Time. Delay Q4, Q5. Time delay Q4, Q5 operates in the same way as time delay Q1, Q2 described in a above, except for a change in the value of charging resistor R9 to achieve a 400-ms time delay before unijunction transistor Q5 is fired.


Figure 3-43. Type XMTR-1B interface transmitter. schematic diagram.


Figure 3-44. Type XMTR-2 interface transmitter, schematic diagram.
c. Rectifier CR1 Through CR4. An input sine wave signal of approximately 3.3 kc is full-wave rectified by diodes CR1 through CR4. The rectified output is filtered by capacitor C 3 to remove high frequency noise.
d. Shaper Q3. A filtered full-wave rectified signal is applied to transistor Q5 which operates as an over


Figure 3-45. Type PHOTO AMPL photocell amplifier, schematic diagram.
driven amplifier to produce output pulses across load resistor R15 at the same frequency as the full-wave rectified input. The signal is then filtered by capacitor C 4 to minimize the high frequency noise.
e. Single Shot Q6, Q7. A positive step input signal switching from 0 volt to +4.5 volts is applied across loading resistor R18 and converted to a sharp positive pulse by differentiator C6 and R19. The positive differentiated pulse is passed by diode CR6 and is applied across loading resistor R22 to drive transistor Q6 into conduction. Transistors Q6 and Q7 form a single-shot multivibrator which produces a positive 140ms output pulse from the collector of Q7.
(1) Initially, Q6 is cut off and Q7 is conducting. The base of Q6 is held slightly below 0 volt by diodes CR5 and CR6 with the aid of current flowing through resistor R22. Base current for Q7 is supplied through resistor R20 and diode CR7. The low level at the collector of Q7 is fed back through resistor R21 to keep Q6 cut off. Initially, capacitor C5 has a a charge of 12 volts since Q6 is cut off.
(2) When the single shot is triggered, Q6 is driven into conduction and supplies a low voltage
through C5 to cut off diode CR7 and transistor Q7. The high output at the collector of Q7 is fed back regeneratively to the base of Q6 through resistor R21 and is applied to the circuit, output across voltage R25, R26. Capacitor C5 charges up through resistor R20 and
transistor R20. After 140 ms , the voltage at the junction of C5 and R20 is sufficiently high to drive CR7 and Q7 into condition, there by terminating the output pulse and driving Q6 into cutoff.

## CHAPTER 4

## MAINTENANCE INSTRUCTIONS

## Section I. GENERAL

## 4-1. Scope of Maintenance

a. This chapter includes instructions for performing preventive and corrective maintenance procedures on all major assemblies, subassemblies, and components (except printed circuit cards) of the card reader. Refer to chapter 5 for information on troubleshooting and repair of the printed circuit cards.
b. Maintenance of the card reader includes the following:
(1) Preventive maintenance para 4-3 through (4-11).
(2) Troubleshooting (para 4-12 through 4-14).
(3) Removal and replacement (para 4-15 through 4-49).
(4) Repairs and adjustments (para 4-50 through 4-69.

## 4-2. Tools, Materials, and Equipment Required

a. Tools and Test Equipment. Refer to appendix C for a list of the tools and test equipment required for maintenance of the card reader.
b. Materials. The following maintenance materials are required in addition to the maintenance materials furnished as part of the tool kits listed in appendix C
(1) Lint-free cleaning cloth, NSN 8305-00267-
3015.
(2) Pressure-sensitive tape.
(3) Fine sandpaper (0000), NSN 5350-00-235-0124.
(4) Lacquer, semigloss, blue (No. 25184, per FED STD 595), NSN 8010-00-721-9753 (1 pt press can).
(5) Enamel, semigloss, gray (No. 26492, per FED STD 595), NSN 8010-00-087-0109 (1 qt can).
(6) Enamel, semigloss, black (No. 27038, per FED STD 595), NSN 8010-00-844-4792 ( $1 \mathrm{qt} \mathrm{can)}$.
(7) Primer, zinc chromate, FED SPEC TTP664, NSN 8010-00-936-3372 (1 pt press can).
(8) Detergent, liquid, NSN 7930-00-926-5280 (pt).
(9) Coater, filter, NSN 4130-00-860-0042 (pt).
(10) Trichloroethane, FED SPEC O-T-620, Type 1, NSN 6810-00-292-9625 (qt), or NSN 6810-00.-664-0387 (gal).
(11) Adhesive (RTV-108), NSN 8040-009147013 ( 2 oz tb ).
(12) Silicone compound (DC-340 heat-sink compound), NSN 6850-00-171-6995 (2 oz tb).
(13) Sealing compound, retaining (LOCTITE, Grade E), NSN 8030-00-081-2328 (50 cc pl btl).
(14) Resistor, fixed, 1,000 ohms, $1 / 4$-watt RC07GF102J), ( 1 ea).
(15) Resistor, fixed, 1,000 ohms, $1 / 2$-watt (RC20GF102J), (1 ea).

## Section II. PREVENTIVE MAINTENANCE

## 4-3. Scope of Preventive Maintenance

a. Preventive maintenance is the systematic care, inspection, and servicing of the card reader to maintain it in serviceable condition, prevent breakdowns, and assure maximum operational capability. Preventive maintenance includes the inspection, testing, and replacement of parts, subassemblies, or units that inspection and tests indicate would probably fail before the next scheduled periodic service.
$b$. The preventive maintenance checks and services charts outline functions necessary to maintain the card reader in good operating condition. The charts indicate what to check, how to check, and what the
normal conditions are; the References column lists the illustrations, paragraphs, or manuals that contain detailed maintenance procedures.
c. Weekly and monthly preventive maintenance periods are specified as follows: A week and a month are defined as approximately 7 and 30 calendar days of 8 -hour-a-day operation, respectively. If the card reader is operated 16 hours a day, the weekly and monthly preventive maintenance checks and services should be performed at 4 -day and 15-day intervals, respectively. Adjustment of the preventive maintenance interval should be made to compensate for any unusual operating conditions.

4-4. Daily Preventive Maintenance Checks and Services Chart

| Sequence No. | Item to be inspected | Procedure | References |
| :---: | :---: | :---: | :---: |
| 1 | Exterior surfaces | Clean the overall cabinet and covers. When cleaning, Para. 4-7]check Para 4-7 for broken, missing, or loose covers, hinges, or hardware. |  |
|  |  |  |  |
| 2 | External cables and co | Inspect external cables and connec kinks, and insecure connections. | of deteriora |

## 4-5. Weekly Preventive Maintenance Checks and Services Chart

| Sequence No. | Item to be inspected | Procedure | References |
| :---: | :---: | :---: | :---: |
| 1 | Drive belts...................... | Check for wear and proper adjustment | Para 4-32b |
| 2 | Picker belts .................. | .Check for wear and height adjustment. | Para 4-54 |
| 3 | Stacker spring .............. | .Check for proper tension . | Para 4-5 |
| 4 | Card reader mechanism. | Clean | Para 4-7 |
| 5 | Blower air filter............. | .Replace.. | None |
| 6 | Muffler ............. | .Empty and clean jar. Clean element. | Para 4-9 |

4-6. Monthly Preventive Maintenance Checks and Services

| Sequence No. | Item to be inspected | Procedure | References |
| :---: | :---: | :---: | :---: |
| 1 | Cabinet | Clean | Para 4-7 |
| 2 | Internal logic area .......... | Clean | Para 4-7 |
| 3 | Picker vacuum relief valve | Check for proper vacuum; adjust if required | Para 4-70 |
| 4 | Picker belts . ............ | Check for wear or deterioration and for proper tension | Para 4-54 |
| 5 | Picker solenoid. | Check for proper adjustment ................................... | Para 4-56 |
| 6 | Blower assembly (B1) |  | Clean if dirty |

## 4-7. Cleaning and Touchup Painting

a. External Cleaning. Use a vacuum cleaner and a lint free cloth to clean all external areas.

## NOTE

A spare blower air filter is required to permit cleaning while the card reader is in use.
b. Card Reader Mechanism. Use a soft brush or low-pressure air to clean dirt, lint, and card dust from the card reader mechanism.
c. Internal Cleaning. Use a vacuum cleaner and a lint free cloth to clean the cabinet and logic section internally.
d. Ball Bearings. All ball bearings used in the card reader are sealed and cannot be cleaned or relubricated. Wipe the exterior of ball bearings with a lint free cloth.
e. Touchup Painting Instructions. Remove rust and corrosion from metal surfaces by lightly sanding them with sandpaper. Brush two coats of paint on bare metal to protect it from further corrosion.

## 4-8. Cleaning Cabinet Air Filter

Remove loose dust and dirt from the cabinet air filter weekly or after each 50 hours of operation, whichever occurs first (and b below). Wash the filter monthly or after each 250 hours of operation, whichever occurs first (c below).
a. Pry the upper corners of the grill assembly forward slightly and lift the grill assembly upward to remove it from the cabinet. Lift the exposed filter upward slightly and then forward to remove it from the equipment cabinet.
b. Use a hand vacuum cleaner to remove loose dust and dirt from both sides of the filter.
c. Wash the filter as follows:
(1) Immerse air filter in a solution of warm water and detergent and move it about to free the dirt. When clean, hang it up to dry.
(2) Hold a spray can of RF Super Filter Coat (Research Products Corp.) about 12 inches from the dry filter and press the button while moving the can to apply an even thin coat to the filter. Then apply an even thin coat to the opposite side of the filter. Repeat this procedure to apply a total of three thin coats to each side of the filter.
d. To install the clean air filter, reverse the removal procedure (a above).

## 4-9. Cleaning of Muffler and Jar Element

a. Unscrew the jar ( $1 \sqrt{\text {, fig. } 4-8}$ ) from the muffler.
b. Unscrew the element (2) from the muffler.

WARNING
The fumes of trichloroethane are toxic. Provide though ventilation whenever used. DO NOT USE NEAR AN OPEN FLAME. Trichloroethane is not flammable, but exposure of the fumes to an open flame or hot metal surfaces forms highly toxic phosgene gases.
c. Clean the element by washing it trichloroethane.
d. Air dry the element with air from a low pressure air source.
e. Replace the element and jar.

4-10. (Deleted)
4-11. Lubrication
Lubrication of the card reader is not required.

## 4-12. Use of Troubleshooting Data

## NOTE

To test the Reader, Punched Card RP152/G, when it is used with the 490-L Overseas AUTOVON, strap terminals 7 and 13 of TB-2.

Troubleshooting information for the card reader is given in the card reader troubleshooting chart (para 4-13). When a particular trouble symptom is observed, the particular trouble or troubles can be corrected by replacing one or more of the components
listed in the checks and corrective measures column. First check resistors, capacitors, relays, and other nonplug-in electrical or mechanical components before replacing the component. Resistance data on transformers, relays, and nonstandard items is given in paragraph 4-14. When a PC card trouble is suspected, check the PC card by substituting al new card. Always recheck the card reader operation after repairs or replacements are performed.

## 4-13. Card Reader Troubleshooting Charts

Locate troubles in the card reader as described in a below. If it is suspected that the trouble is in power supply PS1, refer to b and c below for power supply troubleshooting information.
a. Card Reader Troubleshooting Chart.

Note
When troubleshooting, be alert for loose or damaged connections, short circuits caused by foreign materials, and PC cards that are not securely seated in their connectors.

| Item No. | Trouble symptom | Probable trouble | Checks and corrective measures |
| :--- | :--- | :--- | :--- |

1 Card reader alarm indications:
a. PICK FAIL indicator lights.
a. One or more of following:
(1) Failure to load cards properly
(2) Damaged card
(3) Obstruction in picker throat
(4) Hopper card support out of adjustment.
(5) Picker belt height in need of adjustment.
(6) Picker belts worn smooth
(7) Metering capstan pressure insufficient.
(8) Insufficient vacuum
(9) Pick timer circuit
(10) Control logic
(11) End of card photocell shorted
(12) Solenoid drivers
(13) Photocell amplifiers
(14) Broken metering capstan belt, front or rear.
(15) Broken picker belt set (4 belts)
(16) Broken main drive belt
(17) Broken picker drive belt
(18) Resistor A2A2R1
(19) Picker solenoid A2A2K1
(20) Vacuum pump
a. Proceed as follows:
(1) Remove cards from hopper, and fan and joggle card deck before reloading in hopper.
(2) Remove cards from hopper and check column 1 edge of bottom card for damage.
(3) Check throat for obstructions.
(4) Adjust the hopper card support.
(5) Adjust height of picker belts.
(6) Replace picker belts.
(7) Adjust capstan pressure.
(8) Check for kinks in vacuum line. Clean vacuum line air filter. Adjust vacuum relief valve.
(9) Replace PC card A15.
(10) Replace PC card A16.
(11) Replace photocell.
(12) Replace PC card A1.
(13) Replace PC card A6.
(14) Replace defective belt.
(15) Replace belt set.
(16) Replace belt.
(17) Replace belt.
(18) Replace resistor.
(19) Replace picker solenoid.
(20) If vacuum relief valve adjustment does not provide sufficient vacuum, refer to para. 4-36.1 for repair of vacuum pump. Replace vacuum pump.
(21) Replace hose length.
(21) Vacuum hose
b. One or more of following:
(1) Hopper empty or stacker full .
(2) Hopper photocell defective or shorted
(3) Stacker elevator not descending properly.
(4) Stacker full switch defective .
(5) Photocell amplifiers
b. Proceed as follows:
(1) Take appropriate action.
(2) Replace photocell.
(3) Check for binding. Adjust stacker spring tension.
(4) Replace switch.
(5) Replace PC card A6.

Note. If an alarm is indicated continuously, even when the reader is in a start condition, check lamp driver PC card A3.
c. OUT OF SYNC indicator lights.
c. One or more of following:
(1) Failure to receive end of block signal from CCU.
(2) Interface control card.
(3) Timers and alarm logic card.
(4) Timing generator card.
(5) Photocell amplifier card.
(6) End of card photocell or beginning of card photocell defective.
(7) Faulty card motion
c. Proceed as follows:
(1) Reread card message.
(2) Replace PC card A4.
(3) Replace PC card A15.
(4) Replace PC card A14.
(5) Replace PC card A6.
(6) Replace defective photocell.
(7) Check metering capstan pressure.
Item
No. Trouble symptom
d. CARD JAM indicator lights
e. PHOTOCELL CHECK
f. INVALID CHARACTER indicator lights.
g. Inability to get out of stop condition

2 Incorrect or no alarm or lamp indications:
a. Improper indicator lamp display.
b. Improper panel indicator lamp display.
c. Panel indicator lamps inoperative.
d. All read station lamps and d. HOPPER EMPTY lamp unlighted.
e. Indicator lights at half brilliance.
f. One of two indicators light at half brilliance.
g. AC POWER and-DC POWER indicators not lighted.
(8) Polar interface card
(9) Reluctance pickup A2A4PU 1
(10) Capacitor A2A4C1
d. One or more of following:
(1) Card jammed in read station
(2) Photocell amplifier card
(3) Timing generator card
(4) Timers and alarm logic card
(5) Read station lamps not illuminated.
e. One or more of following:
(1) Photocell amplifier card
(2) Dirt or card piece covering one or more of read station photocell transistors Q1 through Q12.
(3) Timing generator card
(4) Data register card
(5) Code converter
(6) Punch, notch, or other aperature in leading edge of card being read
(7) Photocell transistors Q1 through Q12.
(8) Resistor A2R1
f. One or more of following:
(1) Damaged data processing card or improper punch code.
(2) Photocell amplifier card.
(3) Read station photocell defective
(4) Timing generator card
(5) Invalid character detector card
(6) Data register
g. One or more of following:
(1) Uncorrected alarm condition
(2) No cards loaded
(3) Control logic card
(4) Timers and alarm logic card-
a. Defective lamp (s)
b. Lamp drivers
c. Fuses A10F9 or A10F10

Defective lamp A2A1DS2, resistor A2R1, or lamp A2A1DS1.
e. Lamps A3 DS1 through A3DS9, A3Z2, A3Z6, or A3Z7.
f. Lamp A3Z5
g. One or more of following:
(1) Power supply (PS1) AC or DC fuses.
(2) 15-vac fuses
(3) Lamps defective
(8) Replace PC card A5.
(9) Replace pickup.
(10) Replace capacitor.
d. Proceed as follows:
(1) Remove jammed card.
(2) Replace PC card A6.
(3) Replace PC card A14.
(4) Replace PC card A15.
(5) Replace lamp assembly A2A1DS1. Replace lamp A2A1DS2. Replace resistor A2R1.
e. Proceed as follows:
(1) Replace PC card A6.
(2) Clean out read station.
(3) Replace PC card A14.
(4) Replace PC card A7.
(5) Check PC cards A8, through All, and A13. Replace defective card.
(6) Make new card.
(7) Check and replace defective photocell transistor.
(8) Replace resistor.
f. Proceed as follows:
(1) Replace with correct card.
(2) Replace PC card A6.
(3) Replace defective photocell.
(4) Replace PC card A14.
(5) Replace PC card A8.
(6) Replace PC card A7.
g. Proceed as follows:
(1) Take appropriate action.
(2) Place cards in hopper.
(3) Replace PC card A16.
(4) Replace PC card A15.
a. Replace defective lamp (s).
b. Replace PC card A3.
c. Replace defective fuse.
d. Replace lamp or resistor.
e. Replace defective lamps.
f. Replace lamp.
g. Proceed as follows:
(1) Replace defective fuses.
(2) Replace defective fuses.
(3) Replace defective lamps.

| Item Trouble symptom | Probable trouble | Checks and corrective measures |
| :--- | :--- | :--- | :--- |
| No. |  |  |

3 Data or transmission troubles:
a. One or more field-data invalid characters unrecognized.
b. Transmission error (data) CCU parity error alarm.
c. Transmission errors without alarm.
d. Failure to detect invalid characters.
4 Card functions and motion trouble:
a. Picker solenoid inoperative
b. Card offset failure
c. Uncertain or no card motion into stacker. capstan.
d. Improper offsetting or stacking.
e. Uncertain or no card motion through read station.
f. Drive motor inoperative
g. Picker belts stationary
h. All mechanisms inoperative
a. Solenoid drivers
b. Polar interface card
or ASC11 encorder.
c. One or more of following:
(1) Photocell amplifiers
(2) Data register
(3) Invalid character detector
(4) ASCII encoder
(5) Timing generator
(6) Encode matrix
(7) Decode matrix
d. Invalid character detector or timing generator.
a. One or more of following:
(1) Control logic
(2) Picker solenoid A2A2K1 defective.
(3) Photocell amplifier defective -
(4) End-of-card photocell defective-
(5) Solenoid drivers
(6) Resistor A2A2R1
(7) Resistor A2A2R2
(8) Diode A2A2CR1
(9) Capacitor A2A2C2
b. One or more of the following:
(1) Timing generator and alarm logic
(2) Timers
(3) Resistor A2A3R1
(4) Diode A2A3CR1
(5) Relay A2A3K1
(6) Control logic
(7) Solenoid drivers
c. Offsetting capstan idler or insufficient c. Replace defective part or adjust idler. pressure
d. Offsetting capstan idler or stacker elevator.
e. One or more of following:
(1) Insufficient capstan pull
(2) Broken capstan drive belt, front or rear.
(3) Faulty idler capstan
(4) Faulty drive capstan
f. One or more of following:
(1) Drive motor fuse in power supply.
(2) Relay in power supply
(3) Drive motor
g. Broken picker drive belt, or main drive belt.
h. Faulty drive motor
between offset idler and
a. Replace PC card A1.
b. Replace PC cord A5 or A13
c. Proceed as follows:
(1) Replace PC card A6.
(2) Replace PC card A7.
(3) Replace PC card A8.
(4) Replace PC card A13.
(5) Replace PC card A14.
(6) Replace both PC cards A10 and A12.
(7) Replace both PC cards A9 and A11.
d. Replace PC card A8 or A14.
a. Proceed as follows:
(1) Replace PC card A16.
(2) Replace solenoid.
(3) Replace PC card A6.
(4) Replace photocell.
(5) Replace PC card A1.
(6) Replace resistor.
(7) Replace resistor.
(8) Replace diode.
(9) Replace capacitor.
b. Proceed as follows:
(1) Replace PC card A14.
(2) Replace PC card A15.
(3) Replace resistor.
(4) Replace diode.
(5) Replace relay.
(6) Replace PC card A16.
(7) Replace PC card A1.
d. Adjust offsetting angle of idler or adjust spring tension on elevator.
e. Proceed as follows:
(1) Increase pressure of idler on drive capstan.
(2) Replace capstan drive belt.
(3) Replace idler capstan.
(4) Replace drive capstan.
f. Proceed as follows:
(1) Replace fuse.
(2) Replace relay or drive circuit.
(3) Replace drive motor.
g. Replace belt.
h. Replace drive motor.

| Item | Trouble symptom | Probable trouble | Checks and corrective measures |
| :--- | :--- | :--- | :--- |
| No. |  |  |  |

5 Miscellaneous troubles:
a. Power-on reset malfunction
a. Solenoid drivers
a. Replace PC card A1.
b. Absence of control signal to or from CCU.
c. Card reader will not turn on
d. Alarm condition undetected
e. Improper response to front panel controls.
f. Erratic operation -.
g. Ventilating fan inoperative
h. Damage to cards being read.
i. Damage to cards being read.
b. Control interface
c. One or more of following:
(1) Loss of primary power
(2) AC or DC fuse blown in power supply.
(3) Loss of power connection in unit
(4) AC POWER switch defective
(5) Polar interface
(6) Timing generator and alarm logic
(7) Power supply malfunction
(8) Filter FL1, FL2, FL3, or FL4
d. One or more of following:
(1) Lamp drivers
(2) Timing generator
(3) Control panel lamps
(4) Timers
(5) Photocell amplifiers
e. Control logic
f. One or more of following:
(1) Loose connection in ac power circuit.
(2) Power supply malfunction
(3) Lamp
g. One or more of following:
(1) Fuse A10F7
(2) Faulty blower motor
h. One or-more of following:
(1)Stacker elevator too low
(2) Deflector plate in sticker not lying flat on cards.
(3) One picker belt raised above others.
i. Offset idler
b. Replace PC card A4.
c. Proceed as follows:
(1) Check power source.
(2) Replace blown fuse.
(3) Check for secure connections.
(4) Replace switch.
(5) Replace PC card A5.
(6) Replace PC card A14.
(7) Replace power supply.
(8) Replace defective filter.
d. Proceed as follows:
(1) Replace PC card A3.
(2) Replace PC card A14.
(3) Press LAMP TEST switch to check lamps. Replace defective lamps.
(4) Replace PC card A15.
(5) Replace PC card A6.
e. Replace PC card A16.
f. Proceed as follows:
(1) Check ac power circuit connections.
(2) Check power supply.
(3) Replace lamp.
g. Proceed as follows:
(1) Replace fuse.
(2) Replace blower motor.
h. Proceed as follows:
(1) Adjust stacker spring tension.
(2) Adjust deflector plate.
(3) Adjust picker belt tension.
i. Adjust angle of offset idler.
b. Power Supply PSI, Troubleshooting Procedure.

If there is any malfunction in any of the regulated supplies in power supply PS1, the sequencing module, A12, in the power supply automatically shuts down the entire supply. In order to troubleshoot the power supply, the sequencing module must be removed and in its place a manual control card (Saratoga Industries part No. D39245) must be installed. This control card contains manually operated switches which permit the regulated supplies to be turned on one at a time.
(1) In order to use the manual control card to troubleshoot power supply PS1, first operate all SR of the manual control card. This should turn on all the regulated supplies, which can be monitored at the test jacks on the front of the power supply, as described in paragraph 4-67 (which describes the adjustment procedure for the regulated supplies). If the regulated supplies all go on and are providing outputs within 90 percent of rated value, the malfunction was in the sequencing module A12. If the output voltage of one or more of the regulated
supplies does not meet the required specification, the voltage regulator, or its associated rectifier-filter network is defective, as summarized in the chart (c below). If all regulated supplies are not operating, the ac power transformer (A9T1) is defective or a front panel ac fuse is blown.
(2) If it is suspected that there may be ripple in the output voltage of any one of the regulated supplies, connect an oscilloscope to the output test jacks on the front of the power supply normally monitored by a digital voltmeter (para 4-67). The ac ripple should not exceed the following peak-to-peak values:

| Test point monitored | Maximum ripple (volts, peak to peak) |
| :---: | :---: |
| + 4.75 and COM | 0.01.2 |
| + 12 and COM | 0.02 |
| - 12 and COM | 0.02 |
| - 48 and COM | 0.02 |

(3) If one of the regulated supplies is completely off, check the front panel fuse associated with this supply. If the fuse is not defective, the cause of trouble is in the corresponding voltage regulator card specified in the troubleshooting chart in c below.

## c. Power Supply PSI Troubleshooting Chart.

| Item | Trouble symptom | Probable trouble | Checks and corrective measures |
| :--- | :--- | :--- | :--- |
| No. |  |  |  |

## WARNING

Before removing or installing PC cards or heat sink subassemblies, ensure that input power is removed by opening the main ac input circuit breaker.

1 Power supply shuts off but can be control card is installed.
$2+4.75$-volt output out of tolerance

3 +12volt output out of tolerance

4 -12-volt output out of tolerance

5 -48-volt output out of tolerance
a. +4.75-volt output
b. +12 -volt output
c. - 12-volt output
d. -48 -volt output

Sequencing module PS1A12 defective. Replace module PSIA12.
a. Incorrectly adjusted +4.75-volt regulator.
b. Defective +4.75 volt regulator
c. Defective rectifier-filter network
a. Incorrectly adjusted +12 -volt regulator
b. Defective +12 -volt regulator
c. Defective rectifier-filter network
a. Incorrectly adjusted - 12 volt regulator.
b. Defective-12-volt regulator
c. Defective rectifier-filter network
a. Incorrectly adjusted -48 volt-regulator.
b. Defective 48 -volt regulator
c. Defective rectifier-filter network
a. Adjust +4.7 -volt regulator as dcscribed in paragraph 4-67
b. Replace module PS1A1.
c. Replace heatsink component assembly PS1A4
a. Adjust +12 -volt regulator as described in paragraph 4-67.
b. Replace module PS1A2.
c. Replace heatsink component assembly PS1A5.
a. Adjust -12-volt regulator as described in paragraph 4-67.
b. Replace module PS1A2.
c. Replace heatsink component assembly PS1A5.
a. Adjust -48-volt-regulator as described in paragraph 4-67.
b. Replace module PS1A3 or PS1A6.
c. Replace heatsink component assembly PS1A4.
a. Replace filter capacitor(s).
b. Replace filter capacitor.
c. Replace filter capacitor.
d. Replace defective filter capacitor.
d. Replace defective filter capacitor.

## 4-14. Troubleshooting Reference Data

a. General. When using the dc resistance data listed below, do not use the resistance measurement as the sole basis for determining that the component is defective. Because of broad winding tolerances during
a. Defective filter capacitor A9C2 or A9C3.
b. Defective filter capacitor A9C4
c. Defective filter capacitor A9C5
d. Defective filter capacitor A9C6
manufacture, resistances of operable components may vary considerably.
b. Transformer Windings. The dc resistances of the windings of transformers PS1A9T1 and PS1A12T1 are listed below. The resistances are measured
with all connections removed from the transformer terminals.

| Transformer | Winding terminals | Resistance (ohms) |
| :--- | :---: | :---: |
| PS1A9T1 ................. 1-2 | 0.270 (Max.). |  |
|  | $3-7$ | 0.270 (Max.). |
|  | $4-7$ | 0.021 (Max.). |
|  | $5-7$ | 0.048 (Max.). |
|  | $6-7$ | 0.011 (Max.). |
|  | $7-8$ | 0.011 (Max.). |
|  | $7-9$ | 0.048 (Max,). |
|  | $7-10$ | 0.021 (Max.). |
|  | $7-11$ | 0.270 (Max.). |
|  | $12-13$ | 0.510 (Max.). |
| PS1A12T1 $\ldots . . . . . . . . . . . . . .1-6 ~$ | $1.250(+15 \%)$. |  |
|  | $2-4$ | $0.290(+15 \%)$. |
|  | $3-5$ | $0.370(+15 \%)$. |

c. Solenoid Windings. The dc resistance of the winding of the offset idler solenoid should be approximately 28 ohms. The dc resistance of the picker solenoid winding should be approximately 35 ohms.
d. Additional Reference Data. Illustrations that will help in troubleshooting the card reader are listed below.

## Fig. No. Description

8-1 ...... Color code for marking MIL-STD resistors.
8-2 ...... Color code for marking MIL-STD capacitors.
8-3 ...... Card reader, interconnection, schematic
8-4 ...... diagram.
8-5 ...... Card reader, control panel, schematic diagram.
8-6 ...... Ac circuits, schematic diagram.
8-9 ...... Dc circuits, schematic diagram.
Card reader mechanism assembly A2, schematic diagram.

## Section IV. REMOVAL AND REPLACEMENT

## 4-15. General

The following paragraphs describe the removal and replacement of major assemblies, subassemblies, and components of the card reader. These paragraphs also describe the disassembly and reassembly of major assemblies and subassemblies when not in the order of index numbers on exploded views, or when special tools and procedures are required. Use these procedures in conjunction with the troubleshooting, repair, and adjustment procedures described in paragraphs 4-12, 451, and 4-53, respectively.
a. Removal and Disassembly. Disassemble the card reader only to the extent necessary to inspect, clean, lubricate, and replace a defective part or to adjust the assembly that is in need of maintenance. Open the front or rear door of the card reader inclosure (39, fig. $4-1$ ) as necessary to gain access to assemblies to be removed.
b. Reassembly and Replacement.
(1) Inspect all removed parts for evidence of excessive wear or damage. Install only parts that are unquestionably serviceable.
(2) Check to be sure that mating gears and mechanical linkages are engaged properly before tightening the mounting screws or nuts.

## CAUTION

When securing parts in place, be careful not to tighten the mounting screws or nuts excessively.
(3) Apply sealing compound (SM-B583244008) to the areas indicated by the note on figure 4-1.

## 4-16. Removal and Replacement of Card Reader Mechanism

a. Removal. Remove the card reader mechanism (12, fig. 4-1) in order of index numbers 1 through 11. Remove cables J 1 \& J 2 from the back of the card reader mechanism.

Mechanism cannot be removed without removing cables.
b. Replacement. Replace the card reader mechanism in the reverse order of removal in a above.

## 4-17. Disassembly and Reassembly of Card Reader Mechanism

The disassembly and reassembly of the card reader mechanism is described in paragraphs 4-28 through 449.

## 4-18. Removal and Replacement of Logic Assembly

a. Removal. Remove the logic assembly A1 (15, fig. 4-1) from the card reader as follows:
(1) Pull the logic assembly (15) forward until the latches on the slides lock in the open position.
(2) Remove the four connectors (44, 45, 46, and 47) from A1J1 through A1J4. Disconnect the wiring from terminal blocks A1TB2 and TB3 (26 and 32, fig. 42).
(3) Remove the strain relief bar (113, fig. 4-1) and cable clamps (119, 121, and 122) securing the cables to the logic assembly (15).
(4) Depress the latches on the slides (51, fig. $4-2$ ) and pull the logic assembly from the card reader.
(5) Remove the screws (13 and 14.1) and bar nuts (14) to free the remaining half of slide (51, fig. 4-2 from the card reader inclosure (39, fig. 45-1).
b. Replacement. Replace the logic assembly in the reverse order of removal in a above.

4-19. Disassembly and Reassembly of Logic Assembly A1
(fig. 4-2)
a. Disassembly. Disassemble logic
assembly A1 (15, fiq. 4-1) in the order of the index numbers in figure 4-2
b. Reassembly. Reassemble the logic assembly in the reverse order of index numbers in figure 4-2

4-20. Removal and Replacement of Control Panel A3
a. Removal. Remove the control panel (19, fig. 41) in the order of index numbers 16, 17, and 18.
b. Replacement. Replace the control panel in the reverse order of removal in a above.

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| 1 | Cover assembly |
| :---: | :---: |
| 2 | Hex nut, 3/8 inch |
| 3 | Lockwasher, 3/8 inch |
| 4 | Screw, panhead, 3/8 dia., 7/8 in. long |
| 5 | Washer, 3/8 inch |
| 6 | Mechanism frame |
| 7 | Hex nut, No. 10-32 |
| 8 | Washer, flat, No. 10 |
| 9 | Screw, panhead, No. 10-32, 3/4 in. long |
| 10 | Lockwasher, No. 10 |
| 11 | Safety bracket |
| 11.1 | Card reader |
| 12 | Mechanism assembly A2 |
| 13 | Screw, binding head, No. 10-32, 1/2 in. long |
| 14 | Bar nut, 1/8 inch thick |
| 14.1 | Screw, flat head, No 10-32, 1/2 in. long |
| 15 | Logic assembly A1 |
| 16 | Screw, panhead, No. 8-32, 7/16 in. long |
| 17 | Washer, flat, No. 8 |
| 18 | Lockwasher, No. 8 |
| 19 | Control panel A3 |
| 20 | Power supply PS1 |
| 21 | Screw, hex head, No. 10-32, 9/16 in. long |
| 22 | Lockwasher, No. 10 |
| 23 | Washer, flat, No. 10 |
| 24 | Bar nut, 1/8 inch thick |
| 24.1 | Screw, flat head, No. 10-32, 1/2 in. long |
| 24.2 | Bar spacer |
| 4.3 | Screw, panhead, No. 10-32, 1/2 in. long |
| 24.4 | Angle bracket |
| 24.5 | Hex nut, No. 10-32 |
| 25 | Slide |
| 26 | Screw, panhead, No. 8-32, 1/2 in. long |
| 27 | Washer, flat, No. 8 |
| 28 | Lockwasher, No. 8 |
| 29 | Interface plate assembly |
| 30 | Screw, panhead, No. 10-32 |
| 31 | Shield assembly |
| 31.1 | Standoff |
| 32 | Lockwasher, No. 10 |
| 33 | Filter assembly FL1 |
| 34 | Grill assembly |
| 34.1 | Stud |
| 34.2 | Locknut, No. 6-32 |
| 34.3 | Grill |
| 35 | Screw, panhead, No. 8-32, 7/16 in. long |
| 36 | Washer, flat, No. 8 |
| 37 | Lockwasher, No. 8 |
| 38 | Blower B1 |
| 38.1 | Washable filter |
| 38.2 | Capacitor B1C1 |
| 38.3 | Clockwise blower wheel |
| 38.4 | Counterclockwise blower wheel |
| 38.5 | Blower motor |
| 39 | Card reader enclosure |
| 40 | Control panel wiring harness |
| 41 | Interface plate wiring harness |
| 42 | Cable assembly (W1) |
| 43 | Power distribution cable assy. |
| 44 | Contact assembly P1 (A1J1) |
| 45 | Contact assembly P2 (A1J2) |
| 46 | Contact assembly W1P1 (A1J3) |
| 47 | Contact assembly P3 (A1J4) |
| 48 | Locking screw |
| 49 | Lockwasher, No. 6 |
| 50 | Washer; flat, No. 6 |
| 51 | Insulator |
| 52 | Angle bracket |
| 53 | Keying pin |
| 54 | Screw, flat head, No. 4-40, 5/8 in. long |
| 55 | Hex nut, No. 4-40 |
| 56 | Lockwasher, No. 4 |

Washer, flat, No. 4
Cable clamp
59 Male electrical contad
60 Terminal lug
61 Nameplate
62 Cable strap
63 Cable clamp
64 Chassis
64.1 Rubber bumper

Straight pin
Door
Handle
Cam
69 Rod
Nylon grommet
Mylar liner
72 Right hand door assembly
73 Left hand door assembly
73.1 Rear door
73.2 Cam

74 Rod
75 Mylar liner
76 Rear door assembly
77 Hex nut, No. 10-32
78 Lockwasher, No. 10
79 Washer, flat, No. 10
80 Mounting plate
1 Support plate
Screw, panhead, No. 10-32, 1/2 in. long
Washer, flat, No. 10
84 Lockwasher, No. 10
Shelf
6 Screw, sheetmetal, No. 10
Base
Mounting clip
Horizontal trim
Vertical trim
Screw, flathead, No. 10-32, 3/8 in. long
Hex nut, No. 10-32
Lockwasher, No. 10
Washer, flat, No. 10
Metal logo trim
Logo strip
Reference plate
Drive screw
99 Identification plate
100 Connector (W1P2)
101 Cable clamp
102 Solder ferrule
103 Connector P4
104 Cable clamp
105 Terminal lug
106 Terminal lug
107 Terminal lug
108 Terminal lug
109 Terminal lug
110 Hex nut, No. 10-32
111 Lockwasher, No. 10
112 Washer, flat, No. 10
113 Strain relief bar
114 Screw, panhead, No. 8-32, 5/8 in. long
115 Hex nut, No. 8-32
116 Washer, flat, No. 8
117 Lockwasher, No. 8
118 Lockwasher, external tooth, No. 8
119 Cable clamp
120 Cable clamp
121 Cable clamp
122 Cable clamp
123 Cable clamp
124 Cable clamp
125 Cable clamp
126 Cable support clamp

Figure 4-1 (1). Card reader, component location diagram (part 1 of 3).


Figure 4-1(2). Card reader, component location diagram (part 2 of 3).
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Figure 4-1 (3). Card reader, component location diagram (part 3 of 3).
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Figure 4-2. Logic assembly A1, component location diagram.
Change 4 4-10

Legend fo figure 4-2
PC card A1 (No. A65209-002)
PC card A3 (No. SME 546659)
PC card A4 (No. A65215) Note 2
PC card A4 (No. A65223) Note 2
PC card A5 (No. A65205) Note 1
PC card A5 (No. A65227) Note 2
PC card A6 (No. A52630)
PC card A7 (No. A65145)
PC card A8 (No. A52634)
PC cards A9, A11 (No. A53725)
PC cards A10, A12 (No. A53721)
PC card A13 (No. A52622)
PC card A14 (No. A65149)
PC card A15 (No. A65153)
PC card A16 (No. A65141)
Pin identification overlay
Door latch
Washer, No. 12
Push switch (S1)
Screw panhead, 10-32, 3/4 in. long
Lockwasher, No. 10
Washer, flat, No. 10
Bow handle
Front panel
Panel assembly
Plastic trim
Screw, panhead, 8-32, 3/4 in. long
Lockwasher, No. 8
Nut, hex, No. 8-32
Washer, flat, No. 8
Terminal board (TB2)
Marker strip
Screw, panhead, 6-32, 7/8 in. long
Lockwasher, No 6
Nut, hex, No. 6-32
Washer, flat, No. 6
Terminal board (TB3)
Marker strip
Screw, panhead, 10-32, 5/8 in. long
Lockwasher, No. 10
Washer, flat, No. 10
Hex nut, No. 10-32
Washer, flat, No. 10
Main panel assembly
Screw, nylon, 6-32, 1/2 in. long
Nut, hex, nylon, No. 6-32
Laminated bus (TB1)
Screw, panhead, 6-32, 3/8 in. long
Lockwasher, No. 6
Washer, flat, No. 6
Spacer
Contact plate
Contact plate assembly
PC card insulator
Contact pin
Screw, panhead No. 6-32 5/16 in. long
Connector, insulator
Contact pin (A1J1)
Contact pin (A1J2)
Contact pin (A1J3)
Contact pin (A1J4)
Screw, panhead, 10-32, 1/2 in. long
Nut, hex, No. 10-32
Lockwasher, No. 10
Washer, flat, No. 10
Slide
Chassis
Logic chassis (w/o PC cards)
Chassis assembly
Wiring harness
Terminal lug

4-21. Disassembly and Reassembly of Control Panel
(fig. 4-3)
a. Disassembly. Disassemble the control panel (19, fig. 4-1) in the order of index numbers in figure 4-3.
b. Reassembly. Reassemble the control panel in the reverse order of index numbers in figure 43.

## 4-22. Removal and Replacement of Power Supply PS1

## WARNING

Use two men to remove the power supply (20, fig. 4-1) from the reader inclosure. Use extreme care in handling the power supply (20), to avoid injury to personnel or damage to equipment, since there are no good grasping areas in the rear of these units.
a. Removal. Remove the power supply (20) by sliding out of the reader inclosure on the slides (25) and carefully lifting the power supplies off the slides.

CAUTION
Power unit weighs 70 pounds. This procedure should never be undertaken by less than two persons.
(1) Open the circuit breaker supplying power to the equipment. Even with the unit AC POWER switch in the OFF position, 120 VAC is present at the power supply.
(2) Depress the power supply assembly slide latches and pull the power supply out to the stops on the slide.
(3) Remove the cable clamp on the rear of the power supply which secures the cables connected to the power supply assembly.
(4) Depress the power supply slide latches and pull the power supply forward until it is free of the slide.
(5) Rotate the power supply assembly $180^{\circ}$ in a counterclockwise direction so the bottom of the chassis is facing up.
(6) Replace the power Supply in the slides. Close the power supply far enough to enable the slides to support the assembly. Power can now be applied and the necessary maintenance performed.
(7) To restore the power supply to its operating position, insure the circuit breaker supplying power to the unit is OFF, then reverse the procedures in 1 through 6 above.
b. Replacement. Replace the power supply in the reverse order of removal in a above.

When reinstalling the power supply to the operating position, always rotate power supply in a clockwise direction back to the upright position to prevent twisting the power cables.

4-23. Disassembly and Reassembly of Power Supply
(fig. 4-4)
a. Disassembly. Disassemble the power supply
(20, fig. 4-1 in the order of the index numbers in figure 4-4
b. Reassembly. Reassemble the power supply in the reverse order of the index numbers in figure 4-4

4-24. Removal and Replacement of Interface Plate Assembly
a. Removal. Remove the interface plate assembly (29, fig. 4-1 in the order of index numbers 26, 27, and 28.
b. Replacement. Replace the interface plate assembly in the reverse order of removal in a above.

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TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31
b. Reassembly. Reassemble the interface plate assembly in the reverse order of the index numbers in figure 4-5.
a. Disassembly. Disassemble the interface plate assembly (29, Fig 4-1) in the order of the index numbers in figure 4-5


Figure 4-3. Control panel A3, component location diagram.

| 1 | Indicator light (DS9) |
| :--- | :--- |
| 2 | Indicator light (DS8) |
| 3 | Indicator light (DS7) |
| 4 | Indicator light (DS6) |
| 5 | Indicator light (DS5) |
| 6 | Indicator light (DS4) |
| 7 | Indicator light (DS3) |
| 8 | Indicator light (DS2) |
| 9 | Push switch (Z1) |
| 10 | Indicator light (DS1) |
| 11 | Push switch (Z2) |
| 12 | Push switch (Z3) |
| 13 | Push switch (Z4) |
| 14 | Push switch (Z5) |
| 15 | Push switch (Z6) |
| 16 | Push switch (Z7) |

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11 Push switch (Z2)
12 Push switch (Z3)
13 Push switch (Z4)
14 Push switch (Z5)
15 Push switch (Z6)
16 Push switch (Z7)

Lamp (No. 330)
Panel
Lamp (No. 382)
Hex nut, No. 10-32
Lockwasher, No. 10
Washer, flat, No. 10
Cable clamp
Terminal lug
Terminal lug Jumper

## Legend for figure 4-4

Screw, hex, head, No. 8-32, 3/8 in long
Lockwasher, No. 8
Washer, No. 8
Front Panel Assembly (A10)
Front Panel
Latch
Washer, No. 12
Fuse Holder (XF1)
Fuse Holder (XF4)
Fuse Holder (XF2, XF3, XF9, XF10)
Fuse Holder (XF5, XF7, XF8)
Fuse Holder, (spare)
Fuse, 10 amp, slow blow (F5, F8, and spare)
Fuse, 3 amp, slow blow (F7, F9, F10, and spare)
Fuse, 15 amp , fast blow ( F 1 and spare)
Fuse, 10 amp , fast blow (F2, F3, F4, and spare)
Screw, hex head, No. 10-32, 5/8 in. long
Lockwasher, No. 10
Washer, No. 10
Handle
Test point jack (TP2 throughTP5)
Test point jack (TP1)
Screw, hex head, No. 6-32, 3/8 in. long
Lockwasher, No. 6
Washer, No. 6
Fuse cover
Screw, flathead, No. 6-32, 5/16 in. long
Side plate, left hand
Side plate, right hand
Screw, hex head, No. 8-32, 3/8 in. long
Lockwasher, No. 8
Washer, No. 8
Sequence module bracket, left hand
Sequence module bracket, right hand
Card guide
Screw, hex head, No. 4-40, 1/2 in. long
Lockwasher, No. 4
Washer, No. 4
Hex nut, No. 4-40
Polarization key
Electrical receptacle connector (A9J4)
Sequence module component board assembly (A12)
Screw, hex head, No. 10-32, 4-7/8 in. long
Screw, hex head, No. 10-32, 6 3/8 in. long
Lockwasher, No. 10
Washer, No. 10
Capacitor nest
Insulator
Capacitor, $82,000 \mu \mathrm{ff}, 15 \mathrm{vdc}(\mathrm{A9C2}, \mathrm{A9C3})$
Capacitor, $44,000 \mu \mathrm{f}, 25 \mathrm{vdc}$ (A9C4, A9C5)
Capacitor, $6,700 \mu \mathrm{f}, 100 \mathrm{vdc}(\mathrm{A} 9 \mathrm{C} 5)$
Capacitor, $1,500 \mu \mathrm{f}, 75 \mathrm{vdc}$ (A9C1)
Screw, hex head, No. 6-32, 5/8 in. long
Washer, No. 6
Lockwasher, No. 6
Hex nut, No. 6-32
Screw, pan head, No. 6-32, 3/8 in. long
Capacitor, $9,200 \mu \mathrm{f}, 10 \mathrm{vdcw}$ (A9C7, A9C11)
Capacitor, $4,600 \mu \mathrm{f}, 20 \mathrm{vdcw}$ (A9C8, A9C9)
Capacitor, 1,200 $\mu \mathrm{f}, 75 \mathrm{vdcw}(\mathrm{A} 9 \mathrm{C} 10)$
Capacitor bracket
Screw, hex head, No. 6-32, 3/8 in. long
Lockwasher, No. 6
Washer, No. 6
Heatsink assembly (A11)
End plate
Screw, panhead, No. 6-32, 1/2 in. long
Lockwasher, No. 6
Washer, flat, No. 6
Side cover
Heat sink assembly (A4)
Screw, panhead, No. 6-32, 7/8 in. long
62.8
62.9
62.10
62.11

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78.1
78.2
78.3
78.4
78.5

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81
82
83
83.1
83.2
83.3

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84.1

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Lockwasher, No. 6
Washer, flat, No. 6
Heat sink assembly (A5)
Heat sink assembly (A6)
Screw, hex head, No. 8-32, 3/8 in. long
Lockwasher, No. 8
Washer, No. 8
Relay bracket
Screw, hex head, No. 8-32, 1/2 in. long
Lockwasher, No. 8
Washer, flat, No. 8
Relay, 24 vdc (A9K1)
Grommet
Screw, hex head, No. 6-32, 3/8 in. long
Lockwasher, No. 6
Washer, flat, No. 6
Terminal board bracket
Stiffener
Screw, hex head, No. 6-32, 5/8 in. long
Screw, hex head, No. 6-32, 3/8 in. long
Hex nut, No. 6-23
Shield
Bracket
Shield assembly
Standoff
Lockwasher, No. 6
Washer, flat, No. 6
Terminal board (TB1)
Terminal board (TB2)
Component board assembly (A15)
Screw, hex head, No. 6-32, 5/16 in. long
Lockwasher, No. 6
Washer, flat, No. 6
Spacer
Hex nut, No. 6-32
Screw, hex head, No. 6-32, 3/8 in. long
Lockwasher, No. 6
Washer, flat, No. 6
Connector bracket assembly
Screw, hex head, No. 4-40, 5/16 in. long
Lockwasher, No. 4
Washer, flat, No. 4
Component board assembly (A1)
Component board assembly (A2)
Component board assembly (A3)
Electrical receptacle connector (A9J1, A9J2, A9J3)
Polarization key
Hex nut, No. 10-32
Lockwasher, No. 10
Washer, flat, No. 10
Hex nut, 1/4-20
Lockwasher, No. 1/4 in.
Washer, flat, No. $1 / 4 \mathrm{in}$.
Power transformer (A9T1)
Chassis
Clinch fastener, No. 6-32
Clinch fastener, No. 8-32
Clinch fastener, No. 10-32
Clinch fastener, No. 6-32
Eyelet
Chassis assembly


Figure 4-4. Power supply PS1, component location diagram


Figure 4-5. Interface plate assembly, component location diagram

1. Screw, panhead, 8-32, 1 in. long
2. Nut, hex, No. 8
3. Lockwasher, flat, No. 8
4. Washer, flat, No. 8
5. Jumper plate
6. Terminal board (TB3)
7. Marker strip
8. Screw, panhead, 6-32, 5/8 in. long
9. Hex nut. No. 6
10. Lockwasher, No. 6
11. Alternate jumper
12. Alternate Jumper
13. Terminal board (TB1, TB2)
14. Marker strip
15. Interface plate
16. Screw, panhead, No. 8-32, 5/8 in. long
17. Lockwasher, No. 8
18. Washer, flat, No. 8
19. Cable clamp
20. Terminal lug
21. Ferrule
22. Terminal lug

## 4-26. Removal and Replacement of Filter Assembly

a. Removal. Remove the filter assembly (33, fig. $4-1$ ) in the order of index numbers 30, 31, and 32.
b. Replacement. Replace the filter assembly in the reverse order of removal in a above.

A. FRONT

## 4-27. Disassembly and Reassembly of Filter

 Assembly (fig. 4-6)a. Disassembly. Disassemble the filter assembly ( 33 , fig. $4-1$ ) in the order of the index numbers in figure 4-6.
b. Reassembly. Reassemble the filter assembly in the reverse order of the index numbers in figure 4-6.

Figure 4-6. Filter assembly, component location diagram.

TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31 Legend for figure 4-6

| 1 | Wiring Harness |
| :--- | :--- |
| 2 | Terminal lug |
| 3 | Terminal lug |
| 4 | Terminal lug |
| 4.1 | Terminal lug |
| 5 | Filter (FL3, FL4) |
| 6 | Filter (FL1, FL2) |
| 7 | Screw, panhead, No. 6-32, 7/8 in. long |
| 8 | Hex nut, No 6-32 |
| 9 | Lockwasher, No. 6 |

10 Washer, flat, No. 6
11 Terminal board (FL1TB1)
12
13
4 Terminal lug
4.1 Terminal lug

14
Filter (FL3, FL4)
15
16
17
18
Lockwasher, No. 6
19

Markers strip
Screw, panhead, No. 8-32, 7/8 in. long
Hex nut, No. 8-32
Lockwasher, No. 8
Washer, flat, No. 8
Terminal board (FL1TB1)
Marker strip
Filter plate

# Section V. DISASSEMBLY AND REASSEMBLY OF CARD READER MECHANISM 

## 4-28. General

The disassembly and reassembly of the card reader mechanism is effected by removal and replacement of major assemblies, subassemblies, and components as described in the following paragraphs. These paragraphs also describe the disassembly and reassembly of major assemblies and subassemblies when not in the order of index numbers on exploded views, or when special tools and procedures are required. Use these procedures in conjunction with the
troubleshooting, repair, and adjustment procedures described in paragraphs 4-12. 4-51, and 4-53, respectively.

## 4-29. Removal and Replacement of Muffler

a. Removal. Remove the muffler (41, ig. 4-7) in the order of index numbers $38,40,42$, and 41 .
b. Replacement. Replace the muffler in the reverse order of removal in a above.

## LEGEND FOR FIGURE 4-7

| 12 | Hose clamp |
| :--- | :--- |
| 2 | Hose clamp |
| 3 | Screw, panhead, No. 8-32, 1.2 in. long |
| 4 | Lockwasher, No. 8 |
| 5 | Washer, flat, No. 8 |
| 6 | Tie strap |
| 7 | Filter hose subassembly |
| 8 | Hose fitting |
| 9 | Nut, locking, relief valve |
| 10 | Nut, adjustment, relief valve |
| 11 | Spring, relief valve |
| 12 | Body, relief valve |
| 12.1 | Valve |
| 12.2 | Vacuum relief valve |
| 13 | Vacuum gauge, 0-30 inches Hg. |
| 13.1 | Hose clamp |
| 14 | Vacuum manifold |
| 14.1 | Hose clamp |
| 15 | Tygon tubing |
| 15.1 | Nipple, $1 / 4$ NPT, 1-1/2 in. long |
| 16 | Hex nut, No. 6-32 |
| 17 | Lockwasher, No. 6 |
| 18 | Washer, flat, No. 6 |
| 19 | Screw, binding head, No. $6-32,1 / 2$ in. long |
| 20 | D washer |
| 21 | Hose clamp |
| 21.1 | Screw, binding head, No. $6-32,5 / 16$ in. long |
| 212 | Lockwasher, No. 6 |
| 22 | Connector bracket |
| 23 | Electrical receptacle connector (J3, J4, J5) |
| 23.1 | Contact pin |
| 24 | Screw, binding head, No. 8-32, 1/2 in. long |
| 25 | Lockwasher, No. 8 |
| 26 | Washer, No. 8 |
| 27 | Electrical receptacle connector |
| 28 | Hex nut, 3/8-24 |


| 29 | Magnetic pickup (PU1) |
| :--- | :--- |
| 30 | Socket |
| 31 | Capacitor, 0.033uf, 100 vdcw |
| 32 | Terminal |
| 33 | Bracket |
| 33.1 | Magnetic pickup assembly |
| 34 | Screw, cap, socket head, 1/4-20, 3/4 in. long |
| 35 | Lockwasher, 1/4 in. |
| 36 | Washer, 1/4 in. |
| 37 | Retainer plate |
| 38 | Hose clamp |
| 39 | Hose clamp |
| 39.1 | Stay strap |
| 40 | Tygon tubing |
| 41 | Muffler |
| 42 | Elbow, 90 degree |
| 43 | Pipe plug |
| 44 | Bolt, hex head, 1/4-20, 5/8 in. long |
| 45 | Lockwasher, 1/4 |
| 46 | Washer, 1/4 |
| 47 | Motor assembly, modified |
| 48 | Screw, panhead, No. 10-32, 1-1/2 in. long |
| 49 | Lockwasher, No. 10 |
| 50 | Washer, No. 10 |
| 51 | Standoff |
| 52 | Hex, nut, No. 8-32 |
| 53 | Lockwasher, No. 8 |
| 54 | Washer, No. 8 |
| 55 | Screw, panhead, No. 8-32, 3/4 in. long |
| 56 | Washer, No. 8 |
| 57 | Inlet plate |
| 58 | Gasket |
| 59 | Mixer nozzle |
| 59.1 | Exhauster assembly |
| 60 | Screw, panhead, No. 6-32 5/8 in. long |
| 61 | Lockwasher, No. 6 |
|  |  |


| 61.1 | Straddle plate | 124 | Screw, binding head, No. 4-40, 3/16 in. long |
| :---: | :---: | :---: | :---: |
| 62 | Protector cover | 125 | Lockwasher, No. 4 |
| 63 | Terminal board | 126 | Washer, No. 4 |
| 63.1 | Insulator strip | 127 | Lamp socket |
| 63.2 | Terminal lug | 128 | Input guide |
| 64 | Motor support | 128.1 | Guide-lamp assembly |
| 64.1 | Motor support assembly | 129 | Screw, cap, socket head, 1/4-20, 5/8 in. long |
| 64.2 | Support assembly | 130 | Lockwasher, No. 4 |
| 65 | Belt | 131 | Washer, No. 4 |
| 66 | Belt | 132 | Picker and reader assembly (fig. 4-11) |
| 67 | Screw, cap, socket head, No. 10-32, 1/2 in. long | 133 | Screw, cap, socket head, No. 10-32, 1/2 in. long |
| 68 | Lockwasher, No. 10 | 134 | Lockwasher, No. 10 |
| 69 | Washer, No. 10 | 135 | Washer, No. 10 |
| 70 | Hex. nut, 5/16-24 | 136 | Hex, nut, No. 6-32 |
| 71 | Hex. nut, 5/16-24 | 137 | Lockwasher. No. 6 |
| 72 | Pulley | 138 | Washer, No. 6 |
| 73 | Washer, 3/8 in. | 139 | Lockwasher, external tooth, No. 6 |
| 75 | Pulley | 140 | Screw, binding head, No. 6-32, 5/16 in. long |
| 75 | Spur gear | 141 | Hex. nut, No. 6-32 |
| 76 | Spacer | 142 | Lockwasher, No. 6 |
| 77 | Shaft, stacker capstan | 143 | Screw, binding head, No. 6-32, 3/8 in. long |
| 78 | Roller | 144 | Washer, No. 6 |
| 79 | Ball bearing | 145 | Lockwasher, external tooth, No. 6 |
| 80 | Sleeve | 146 | Bonding strap |
| 81 | Ball bearing | 147 | Retaining ring |
| 82 | Offset driver support | 148 | Pivot pin |
| 82.1 | Offset drive assembly | 149 | Card deflector |
| 83 | Screw, binding head, No. 8-32, 3/4 in. long | 150 | Screw, binding head, No. 8-32, 3/8 in. long |
| 84 | Lockwasher, No. 8 | 151 | Washer, No. 8 |
| 85 | Washer, No. 8 | 152 | Roller shaft |
| 86 | Spacer | 153 | Ball bearing |
| 87 | Spacer | 154 | Ball bearing |
| 88 | Electrical plug connector (A2P1) | 155 | Roller |
| 89 | Return spring | 156 | Retaining ring |
| 90 | Hex. nut, No. 6-32 | 157 | Offset idler spring |
| 91 | Lockwasher, No. 6 | 158 | Washer |
| 92 | Washer, No. 6 | 159 | Pivot frame assembly |
| 93 | Guard cover | 160 | Screw, binding head, No. 10-32, 1 1/8 in. long |
| 94 | Standoff | 161 | Lockwasher, No. 10 |
| 95 | Bumper | 162 | Washer, No. 10 |
| 96 | Solenoid plunger | 163 | Nut strip |
| 97 | Hex. nut, No. 5-40 | 164 | Pivot arm pin |
| 98 | Screw, binding head, No. 6-32, 3/8 in. long | 165 | Pivot arm |
| 99 | Lockwasher, No. 6 | 166 | Screw, binding head, No. 4-10, 5/16 in. long |
| 100 | Washer, No. 6 | 167 | Lockwasher, No. 4 |
| 101 | Screw, binding head, No. 8-32, 1/2 in. long | 168 | Solenoid |
| 102 | Lockwasher, No. 8 | 169 | Solenoid bracket |
| 103 | Washer, No. 8 | 170 | Screw, binding head, No. 4-40, 1 in . long |
| 104 | Solenoid stop | 171 | Lockwasher, No. 4 |
| 105 | Solenoid | 172 | Washer, No. 4 |
| 106 | Screw, binding head, No. 4-40, 1/4 in. long | 173 | Component cover |
| 107 | Lockwasher, No. 4 | 174 | Standoff |
| 108 | Resistor (A1R2) | 175 | Screw, binding head, No. 4-40, 3/8 in. long |
| 109 | Hex. nut. No. 6-32 | 176 | Lockwasher, No. 4 |
| 110 | Washer, No. 6 | 177 | Resistor (A1R1) |
| 111 | Continuous thread stud | 178 | Diode (A1CR1) |
| 112 | Diode (CR) | 179 | Electrical contact |
| 113 | Resistor, 2700 ohms, I watt | 180 | Electrical plug connector (A3P1) |
| 114 | Capacitor (A1C1) | 181 | Stud terminal |
| 114.1 | Mounting clip | 182 | Screw, binding head, No. 10-32, 5/8 in. long |
| 115 | Stud terminal | 183 | Lockwasher, No. 10 |
| 116 | Electrical contact | 184 | Washer, No. 10 |
| 117 | Component board | 185 | Support |
| 118 | Electrical shield plate | 186 | Screw, binding head, No. 2-56, 1/2 in. long |
| 119 | Picker solenoid bracket | 187 | Lockwasher, No. 2 |
| 119.1 | Solenoid assembly | 188 | Washer, No. 2 |
| 120 | Screw, binding head, No. 8-32, 1/2 in. long | 189 | Nut strip |
| 121 | Lockwasher, No. 8 | 190 | Push switch (S1) |
| 122 | Washer, No. 8 | 191 | Screw, binding head, No. 10-32, 7/8 in. long |
| 123 | Lamp (DS1) | 191.1 | Locknut, No. 10-32 |



Figure 4-7. Card reader mechanism, exploded view.

## 4-30. Removal and Replacement of Magnetic Pickup Assembly

a. Removal. Remove the magnetic pickup assembly (33.1, figure 4-7) in the order of index numbers 24, 25, and 26. Remove plug A2P1.
b. Replacement. Replace the magnetic pickup assembly in the reverse order of removal in a above. After replacement, perform the ad[justment procedure described ir paragraph 4-59.

## 4-31. Disassembly and Reassembly of Magnetic Pickup Assembly

a. Disassembly. Disassemble the magnetic pickup assembly in the order of index numbers 27 through 33 in figure 4-7.
b. Reassembly. Reassemble the magnetic pickup assembly in the reverse order of disassembly in a above.

## 4-32. Removal and Replacement of Motor and Support Assembly

a. Removal. Removal of the motor and support assembly ( 38 through 64, fig. 4-7) requires two men due to the weight of the assembly.
(1) Disconnect and tag the motor leads at the terminal board (63, fig. 4-7).
(1.1) Remove hose clamp (14.1) and tygon tubing (15).
(1.2) Remove hose clamp (1) and filter hose subassembly (7).
(2) Hold assembly in place and remove mounting screws (34), lockwasher (35), flat washer (36), and retainer plate (37).
(3) Lower assembly and unhook drive belt (66) from pulley (15, fig. 4-10).
b. Replacement. Replace the motor and support assembly in the reverse order of removal in a above except as follows: Before fully tightening the mounting screws (34, fig. 4-7), raise the assembly so that the drive belt (66) is not slack, then tighten the mounting screws. Although the drive belt tension is not critical, the drive belt should not be so loose that there is play, or so tight that the pulley bearings bind.

## 4-33. Disassembly and Reassembly of Motor and Support Assembly

a. Disassembly. Disassemble the motor and support assembly in the order of index numbers 18 through 64 in figure 4-7.
b. Reassembly. Reassemble the motor and support assembly in the reverse order of disassembly in a above.
4-34. Disassembly and Reassembly of Muffler
a. Disassembly. Disassemble the muffler (41 fig. 4-7) in the order of the index numbers in figure 4-8.
b. Reassembly. Reassemble the muffler in the reverse order of disassembly in a above.

## $4-35$. Deleted

4-36. Disassembly and Reassembly of Motor and Pump
a. Disassembly. Disassemble the motor and pump (47, fig. 4-7) in the order of the index numbers in figure 4-10.
b. Reassembly. Reassemble the motor and pump in the reverse order of disassemble in a above.
4-36.1.

## Vacuum Pump Vane Replacement NOTE

If a minimum of 5 inches Hg cannot be obtained after cleaning muffler, checking vacuum lines, and adjustment of vacuum relief valve (para 4-70), the vanes in the vacuum pump may require replacement.

Replace vanes in the vacuum pump as follows:
a. Remove screws (1, fig. 4-10) and washers (1.1) while supporting end plate (2). Remove end plate (2).
b. Remove worn carbon vanes (5) and clean carbon particles from the pump.
c. Insert new carbon vanes (5) with raised edge facing toward the outside and toward the direction of rotor rotation.
d. Replace end plate (2) and secure with screws (1) and washers (1.1).
e. Allow drive motor to operate for approximately 30 minutes, then readjust vacuum relief valve as outlined in paragraph 4-70.

## 4-37.Removal and Replacement of Offset Drive Assembly

a. Removal. Removal of the offset drive assembly (70 through 82, fig. 4-7) results in the disassemble of the assembly.
(1) Remove belt (65, fig. 4-7), by sliding off flangeless pulley (55, fig. 4-11).
(2) Remove motor and vacuum pump (para 432 to gain access to drive assembly pulleys.
(3) Remove the two nuts ( 70 and 71, fig. 4-7 from the shaft (77). Since there is no convenient place for holding the shaft, only one of the nuts (70 or 71) may come off.
(4) All components on the shaft are held in place by compression of the two nuts. If the rear nut (70) has been removed in step (3), slide pulley (72), washer (73), pulley (74), spur gear (75), and spacer (76) off the shaft from the rear of the panel.

## NOTE

On some units, pulleys (72 and 74) and spur gear (75) may have setscrews which must be loosened.

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(5) Remove shaft (77) from the front, grasping roller (78), and sleeve (80) as they come free.
(6) If the front nut (71) was removed in step (3), remove shaft ( 77 complete with pulleys and washers from the rear of the panel grasping roller (78) and sleeve (80) as they come free. Then remove the remaining parts identified in step (4) from the shaft (77).
(7) Remove screws (67), lockwashers (68), and flatwasher (69) to release offset driver support (82).
(8) Remove bearings (79 and 81) from the offset driver support (82).
b. Replacement.
(1) Set bearings (79 and 81) into the support (82).
(2) Hold roller (78) in support (82) and insert shaft (77).
(3) Place nut (71) on shaft (77) and tighten.
(4) Slip spacer (80) onto other end of shaft (77).
(5) Attach support (82) to panel with screws (67), lockwashers (68), and flat washers (69), but do not tighten.
(6) Slide spacer (76) onto shaft from rear, then assemble spur gear (75), pulley (74-larger than pulley 72), washer (73), and pulley (72) onto shaft (77).
(7) Replace nut (70) and tighten to 10 footpounds torque while holding nut (71).
(8) Hook belt (66) over pulley (74) and let hang loose.
(9) Hook belt (65) over pulley (72) and slide over flangeless pulley (55, fig. 4-11.

## NOTE

On units having setscrews in pulleys (72 and 74) and spur gear (75), tighten setscrews.
(10) Position support (82) so that belt (65) will deflect $1 / 4$ inch when 1 pound of force is applied at the center of its span, then tighten screws (67).
(11) Replace motor and vacuum pump and hook belt (66) over motor drive pulley as described in paragraph 4-32

NOTE
Element, muffler assembly, NSN 4310-00-957-1967 is composed of items s 2, 3, 4, 7, and 8 .


Figure 4-8. Muffler, exploded view.

1 Jar
2 Muffler element
3 Muffler plate
4 Body
5 Gasket
6 Cover

7 Stud
8 End cap
9 Coupling

4-38. Removal and Replacement of Picker Solenoid Assembly
a. Removal.
(1) Before removing mounting hardware, remove parts bearing index numbers 88 through 93 in figure 4-7.
(2) Remove picker solenoid assembly (88 through 119, fig. 4-7) in the order of index numbers 83 through 87.
b. Replacement. Replace the picker solenoid assembly in the reverse order of removal in a above. After replacement, perform the adjustment procedure described ir paragraph 4-56.

## 4-39. Disassembly and Reassembly of Picker Solenoid Assembly

a. Disassembly. Disassemble the picker solenoid assembly in the order of index numbers 94 through 119 in figure 4-7
b. Reassembly. Reassemble the picker solenoid assembly in the reverse order of disassembly in a above.

## 4-40. Removal and Replacement of Input Card Guide and Lamp Assembly

a. Removal.
(1) Remove terminal cover (238, fig. 4-7 and disconnect and tag wires from terminal board TB2 (243).
(2) Remove the input card guide and lamp assembly (123 through 128, fig. 4-7) in the order of index numbers 120, 121, and 122 in figure 4-7.
b. Replacement. Replace the input card guide and lamp assembly in the reverse order of removal in a above. After replacement, perform the adjustment procedure described in paragraph 4-58.

## 4-41. Disassembly and Reassembly of Input Card Guide and Lamp Assembly

a. Disassembly. Disassemble the input card guide and lamp assembly in the order of index numbers 123 through 128 in figure 4-7.
b. Reassembly. Reassemble the input card guide and lamp assembly in the reverse order of disassembly in a above.

4-42. Removal and Replacement of Picker and Read Assembly
a. Removal.
(1) Remove wiring race (258,fig. 4-7).
(2) Remove photocell assembly (44.1, fig. 4-
11) and let it rest on the safety bracket so that no undue stress is placed on the wires.
(3) Disconnect and tag leads of the light station assembly (9, fig. 4-11), and hopper empty lamp (127, fig. 4-7, from TB2.
(4) Remove input guide (128 fig. 4-7).
(5) Disconnect and tag leads No. 9 and 10 of terminal board TB1 for hopper empty photocell (47, fig. 4-11.
(6) Loosen hose clamp (13.1, fig. 4-7) and remove tygon tubing (15, fig. 4-7) from the air transmitter throat ( 33 , fig. 4-11) of the picker assembly.
(7) Remove spring (89, fig. 4-7) from the picker assembly.
(8) Loosen hose clamp (2, fig. 4-7) and remove hose from the vacuum tube. Picker assembly will lift out with the vacuum tube in its present position.
(9) Slide belt ( 65 , fig. 4-7) from the pulley (55, fig. 4-11.
(10) Loosen setscrews (54, fig. 4-11) and remove pulley.
(11) Remove picker and read assembly (132, fig. 4-7) by removing three screws (129), three lockwashers (130), and three flat washers (131).
b. Replacement. Replace the picker and read assembly in the reverse order of removal in a above. After replacement, perform the adjustment procedures described in paragraphs 4-32 b, 4-56, 4-57, 4-58, 4-59, and 4-70.

## 4-43. Disassembly and Reassembly of Picker and Read Assembly

a. Disassembly. Disassemble the picker and read assembly in the order of the index numbers in figure 411 , noting the following:

## WARNING

Use care when removing glass cover so as not to cut the hands.
(1) Remove glass cover (7, 43, and 45), only if the glass is broken, cracked, or scratched, by separating the glass from the surface to which it is glued. Remnants of glass which stick may be removed with a single-edge razor blade. Remnants of adhesive which stick may be removed by rubbing with a pencil eraser.
(2) Do not lose or interchange shims $(16,22)$ between the idler arms $(19,25)$ and the light station platform (26); or the shims (13) between the two idler arms (19, 25).
(3) Bearings (18 and 24) must be pressed out of idler arms (19 and 25).
(4) Remove pulleys (49 and 58) simultaneously, with belts (53 and 56) still in place, then remove belts from pulleys.

## NOTE

On later assemblies, only one setscrew (48) is used.
(5) Bearings (50) must be pressed out of picker frame (80).
b. Reassembly. Reassemble the picker and read assembly in the reverse order of the index numbers in figure 4-11, noting the following:
(1) To replace glass covers (7, 43, and 45), apply a thin even layer of adhesive, General Electric part No. RTV-108, or equivalent, on each side of the apertures and set the glass in place. Press the glass onto the adhesive, using a piece of cloth or cotton and firm finger pressure. Make sure glass does not protrude above adjacent surfaces and allow adhesive to dry for 15 minutes before replacing part to which glass cover is attached.
(2) Shims $(16,22,13)$ must be reinstalled in the same location they occupied before disassembly. THEY MUST NOT BE INTERCHANGED. The shims control the position of the idler roller with respect to the drive rollers. The idler rollers must be within flush to 0.010 inch under flush with respect to the inboard edge of the drive rollers.
(3) The four picket belts (66) must be replaced as a matched set.
(4) Hook belts (53 and 56) over pulleys (49 and 58) and slide pulleys onto shafts (51.1 and 62) simultaneously. Mount self-locking nuts (47.1) on the
roller assemblies (52) and use a torque wrench to tighten the nuts to a torque of 6 foot pounds.
(5) Press bearings (50) into picker frame (80).
(5.1) When replacing light station assembly (9) and photocell assembly (44.1), press each bracket against its respective mounting surface while tightening screws.
(6) When replacing photocell semiconductor devices (37), make sure they are fully seated in their slots. After all photocells are in place, tighten screws (34) until they hit their stops.
(7) Perform the picker belt adjustment (para 4-54 after completing reassembly.
(8) Perform metering capstan pressure adjustment (para 4-55).
(8.1) Check the positioning of throat block (29, fig. 4-1) by placing a card in the picker assembly. Push card flush with rear of picker bed and slide it up to the throat block. The leading edge of the card should contact the throat block squarely. If not, loosen screws (27) and reposition throat block (29).
(9) Deleted.
(10) Deleted.

Figure 4-9. Deleted.


Figure 4-10 (1). Motor and pump, exploded view (part 1 of 2)


Figure 4-10 (2). Motor and pump, exploded view (part 2 of 2).

| 17 | Rotor |
| :--- | :--- |
| 18 | Mechanism |
| 19 | Front end housing |
| 19.1 | Bearing |
| 20 | Switch |

21 Stator
22
23
24 Motor-pump assembly
25 Filler plug

Terminal lug
Terminal lug


Figure 4-11. Picker and read assembly, exploded view.

| 1 | Setscrew, cup point, No. 6-32, 3/16 in. long |
| :--- | :--- |
| 2 | Vacuum tube |
| 3 | Shoulder screw, 5/16 OD, 1 1/4 in. long |
| 4 | Screw, binding head, No. 10-32, 1/2 in. long |
| 5 | Lockwasher, No. 10 |
| 6 | Washer, No. 10 |
| 7 | Glass cover |
| 8 | Lug terminal |
| 9 | Light station assembly |
| 9.1 | Spring pin |
| 10 | Spring plunger |
| 11 | Setscrew, flat point, No. 8-32, 3/16 in. long |
| 12 | Pivot shaft |
| 13 | Shim, 0.003 in. thick |
| 14 | Retaining ring |
| 14.1 | Card roller |
| 14.2 | Roller shaft |
| 15 | Card roller assembly |
| 16 | Shim, 0.005 in. thick |
| 17 | Bushing bearing |
| 18 | Ball bearing |
| 18.1 | Arm subassembly |
| 18.2 | Idler arm assembly |
| 19 | Idler arm |
| 20 | Retaining ring |
| 20.1 | Card roller |
| 20.2 | Roller shaft |
| 21 | Card roller assembly |
| 22 | Shim. 0.010 in. thick |
| 23 | Bushing bearing |
| 24 | Ball bearing |
| 24.1 | Arm subassembly |
| 24.2 | Idler arm assembly |
| 25 | Idler arm |
| 26 | Light station platform |
| 26.1 | Light station and roller assembly |
| 27 | Screw, cap, socket head, No. 10-32, 3/8 in. long |
| 28 | Lockwasher |
| 29 | Throat block |
| 30 | Screw, binding head, No. 8-32, 1/2 in. long |
| 31 | Lockwasher, No. 6 |
| 32 | Washer, No. 6 |
| 33 | Air transmitter throat |
| 34 | Screw, binder head, No. 4-40, 3/4 in. long |
| 34 | Lockwasher, No. 4 |
| 37 | Whasher, No. 4 |
|  | Photocell semiconductor device (1Q1 through 1Q14) |

## 4-44. Removal and Replacement of Offset Idler Roller Assembly

a. Removal.
(1) Disconnect connector (180 fig. 4-7).
(2) Disconnect and tag leads at switch S1 (190).
(3) Remove two screws (133, lockwashers (134), and washers (135) which secure the offset idler roller assembly ( 136 through 198) to the panel and remove the offset idler roller assembly.
b. Replacement. Replace the offset idler roller assembly in the reverse order of removal in a above observing the following special procedures:
(1) When replacing deflector bracket (198, fig. 4-7) position the bracket to allow approximately

Legend for figure 4-11
38 Electrical contact
38.1 Photocell assembly

39 Insert
40 Screw, binding head, No. 10-32, 7/8 in. long
41 Lockwasher, No. 10
42 Washer, No. 10
43 Glass cover
44 Angle bracket
44.1 Photocell assembly

45 Glass cover
46 Setscrew, flat point, No. 6-32, 3/16 in. long
47 Photocell assembly
47.1 Nut, self-locking

48 Setscrew, flat point, No. 8-32, 3/16 in. long
49 Pulley
50 Ball bearing
51 Roller
1.1 Roller shaft

Roller assembly
Positive drive belt
Setscrew, flat point, No. 10-32, 3/8 in. long
Pulley
Positive drive belt
Setscrew, flat point, No. 8-32, 3/16 in. long
Pulley
Ball bearing
Setscrew, flat point, No. 8-32, 3/16 in. long
Drive pulley
Picker drive shaft
Spring plunger
Slider
4.1 Retaining ring

Bearing
Belt set, picker
Idler pulley
Idler shaft
Screw, binding head, No. 4-40, 3/8 in. long
Lockwasher, No. 4
Washer, No. 4
Positioning plate
Setscrew, cup point, No. 8-32, 3/16 in. point
Pivot shaft
Drive pin, $3 / 32$ dia, $1 / 2 \mathrm{in}$. Ig.
Belt pusher
Screw, flathead, No. 4-40, 5/16 in. long
Guide spring
Nut plate
Picker frame
$1 / 16$ inch clearance between the elevator assembly backer plate (217) and the reader panel (282).
(2) After replacement, perform the adjustment procedures described in paragraphs 4-60, 461, 4-62, and 4-65.

## 4-45. Disassembly and Reassembly of Offset Idler Roller Assembly

a. Disassembly.
(1) Unsolder and tag solenoid leads at terminal posts (181,fig. 4-7).
(2) Partially disassemble the assembly in the order of index numbers 136 through 155 in figure 4-7.
(3) Remove retaining ring (156).
(4) Spring (157) is in torsion. Grasp the ends of the spring with the fingers to hold it in torsion and slide out pivot frame assembly (159).
(5) Slowly release torsion on spring (157) and remove the spring and spacer (158).
(6) Remove remaining parts in the order of index numbers 160 through 198 in figure 4-7.
b. Reassembly.
(1) Reassemble part of the assembly in the reverse order of index numbers 160 through 198 in figure 4-7.
(2) Place washer (158) in position on pivot frame assembly (159).
(3) Grasp the ends of spring (157) and squeeze it to put it in torsion.
(4) Place the spring in position and slide the long part on pivot frame (159) up through the center of the spring and through the hole in support (185). Make sure that the small post on pivot frame (159) engages the pivot arm (165).
(5) Hook one end of spring (157) over the edge of solenoid bracket (169) and allow the other end of the spring to rest against the face of the arm on pivot frame (159).
(6) Install retaining ring (156) onto the long shaft of the pivot frame as close to the top as possible.
(7) Reassemble the remaining parts of the assembly in the reverse order of index numbers 136 through 155 in figure 4-7.

## 4-46. Removal and Replacement of Elevator Assembly

a. Removal.
(1) Loosen setscrew (202, fig. 4-7), remove collar (203), and remove hangar (204) and spring (205).
(2) Remove two screws (206) securing retainer clip (207) and remove the retainer clip.
(3) Remove two screws (199), lockwashers (200), and washer (201) at each end of shaft (212).
(4) Loosen setscrew (208) and slide shaft (212) out of assembly from rear of panel.
(5) Remove the elevator assembly (202 through 217) from the front of the panel by lowering the

## Section VI. REPAIR AND ADJUSTMENTS

## 4-50. General

This section contains repair instructions, adjustment procedures, and tolerance requirements for the card reader.

## 4-51. Repair

Repair normally consists of removing and replacing a defective part as described in the removal and given in sections IV and V.

## 4-52. Spring Data

elevator to the bottom of its travel and moving it to the left.
b. Replacement. Replace the elevator assembly in the reverse order of removal in a above observing the following special procedures.
(1) When replacing the screws (199) securing shaft (212), position the shaft (212) to allow approximately $1 / 16$ inch clearance between the backer plate (217) and the reader panel (282). It may be necessary to loosen screws (182) so the deflector bracket (198) may be repositioned to prevent roller (193) from interfering with this requirement.
(2) After replacement, perform the adjustment procedures described in paragraphs 4-63, 464, and 4-65.

## 4-47. Disassembly and Reassembly of Elevator Assembly

a. Disassembly. Disassemble the elevator assembly in the, order of index numbers 202 through 217 in figure 4-7.
b. Reassembly. Reassemble the elevator assembly in the reverse order of disassembly in a above.

## 4-48. Removal and Replacement of Top and Bottom Card Guides

a. Removal. Remove the top and bottom card guides (221 and 222, fig. 4-7) in the order of the index numbers 218, 219, and 220.
b. Replacement. Replace the top and bottom card guides in the reverse order of removal in a above. After replacement, perform the adjustment procedure described ir paragraph 4-62.

## 4-49. Removal and Replacement of Card Input Support

a. Removal. Remove the card input support (226, fig. 4-7) in the order of index numbers 223, 224, and 225.
b. Replacement. Replace the card input support in the reverse order of removal in a above. After replacement, perform the adjustment procedure described ir paragraph 4-66.
replacement or disassembly and reassembly procedures

Use the following data to determine whether a spring meets the tension or compression requirement and also as a means of identifying springs. Replace all springs which do not meet the
tension, compression, or torsion tensions requirements.
a. Picker Solenoid Spring. The picker solenoid spring (89, fig. 4-7) is shown in part A of figure 4-12.

The force required to stretch the spring to its extended length is $2( \pm .2)$ pounds.
b. Stacker Elevator Spring. The stacker elevator spring (205, fig. 4-7) is shown in part B of figure 4-12. The force required to stretch the spring to its extended length is 5.5 ( $\pm .4$ ) pounds.
c. Offset Idler Spring. The offset idler spring (157, fig. 4-7) is shown in part C of figure 4-12. Replace the spring when it is too weak to restore the offset idler roller assembly to the non-offset position fig. 3-8.

## $4-53$. Adjustments

The adjustment procedures described in the following paragraphs are arranged in the proper sequence for a complete readjustment of the card reader. When making individual adjustments, check all related adjustments. When removal of parts or subassemblies is necessary to make an adjustment, reference is made to specific paragraphs for removal and replacement.

## 4-54. Adjustment of Picker and Stacker Capstan Shaft Belt Tension

(fig. 4-7, and 4-13)

## Note.

See para 4-32b for tension requirements of the stacker capstan belt (item 66).
a. Requirement. The picker belt idler pulley must rotate freely and without binding. The two belt tension springs must be set at $5 \pm 1$ pounds and be within $1 / 4$ pound of each other.
b. Method of Checking. Place the probe of a pushtype spring scale against each spring-loaded plunger, and press until a small movement of the slider block is noted, so as to relieve some belt tension. Read the spring scale at this point. Repeat for each plunger.
c. Adjustment. Use an Allen wrench to rotate the spring-loaded plunger in the slider blocks. Clockwise rotation increases tension and counterclockwise rotation decreases tension. (Ref. para 4-42 for removal and replacement of picker \& read assembly. This assembly must be removed to perform the adjustment.)

## 4-55. Adjustment of Metering Capstan Pressure (fig.

 4-14)a. Requirement. The metering capstan pressure must be such that a $21 / 2$-pound pull is applied to a card at the inboard capstan and idler (adjacent to panel) and a 3-pound pull is applied to a card at the outboard capstan and idler.

## b. Method of Checking.

(1) Cut a standard punched card lengthwise between card rows 3 and 4. Reinforce one end of onehalf of the card with pressure-sensitive tape on both sides, and punch a hole through which the spring scale can be hooked.
(2) Remove the card input support (para 449).
(3) Insert the untaped end of the card between the inboard capstan and idler.
(4) Hold the inboard capstan pulley with one hand and pull the free end of the card with the spring scale to measure the force required to pull the card out. The required force should be $21 / 4 \pm 1 / 4$ pounds.
(5) Repeat steps (3) and (4) above for the outboard capstan and idler. The required force should be $23 / 4 \pm 1 / 4$ pounds.
(6) Replace the card input support (para 449).
c. Adjustment. Rotate the inboard capstan adjusting screw to adjust the inboard capstan pressure and rotate the outboard capstan adjusting screw to adjust the outboard capstan pressure. Clockwise rotation of the screws increases pressure and counterclockwise rotation decreases pressure.

## 4-56. Adjustment of Picker Solenoid (fig. 4-15)

a. Requirement. When the picker solenoid is energized, the picker belts should protrude through the slots in the picker plate a maximum of one belt thickness and a minimum of $1 / 2$ belt thickness. When the picker solenoid is deenergized, the belts should fall below the picker plate 0.015 to 0.030 inch.
b. Method of Checking. With the hopper

A. picker solenoid spring



C. offset idlea spaing

Figure 4-12. Spring dimensions.


Figure 4-13. Picker belt tension requirement.
empty, use a feeler gauge to check the distance between the top of the belts and the picker plate; then manually actuate the picker solenoid, and observe the movement of the four belts through the slots in the picker plate.
c. Adjustment. Manually actuate the picker solenoid while the belts are not running. Loosen the jam nut, and rotate the long nut to extend or shorten the plunger. If the requirement cannot be obtained in this manner, the entire solenoid assembly can be repositioned slightly by loosening the two solenoid bracket attaching screws. Panel holes for these screws are slightly oversized to permit adjustment.

## 4-56.1. Adjustment of Picker Throat Clearance

a. Requirement. A . 010 inch thick oil feeler gauge should slide under the plate on the throat mounting blocks with some slight resistance. This clearance should be present on both sides of the plate.
b. Method of Checking. With the .010 inch oil feeler gauge, check picker throat clearance by placing the gauge under the plate on the throat mounting blocks. Check clearance on both sides of the plate. Clearance should be such that the feeler gauge slides under the plate with some slight resistance.
c. Adjustment.
(1) Adjustment procedure for pickers with adjustment screws:
(a) If clearance is improper, adjust clearance by first loosening the Allen screws which hold the throat mounting block secure.
(b) Adjust the clearance by turning the remaining four $1 / 16$ inch Allen screw on the throat mounting block.
(c) After adjusting, secure the throat mounting block.
(2) Adjustment ,procedure for picker throat clearance on pickers without Allen adjustment screws:
(a) Loosen the two Allen screws on the picker throat mounting block.
(b) Vary the throat clearance by placing shims under the throat mounting block. To increase clearance, place shim stock ( $1 / 2$ inch square) behind each of the mounting screws in the block (area closest to picker belts). If clearance is to be decreased, the shim stock must be placed in front of the mounting screws (area closest to the mouth of the head).
(3) Check throat clearance; ensure that the clearance is even throughout.
(4) Tighten the throat mounting Allen screws.

## 4-57. Adjustment of Read Station Phototransistor

 (fig 4-16)a. Requirement. The 14 read station phototransistors must be correctly positioned in their mounting block for maximum response.

## b. Method of Checking.

(1) Set the oscilloscope input voltage selector to the 1 -volt position and connect the oscilloscope probe to the 14 inverter outputs HOL1 through HOL12, BC, and EC (fig. 8-14).
(2) Check to assure there are no cards in the hopper, turn on the reader and verify all lamps on the light station are lighted.
(3) Using a card to block the lamps, check the voltage output of each of the 14 inverters for the covered and uncovered condition. The dc voltage level should be between +4.0 volts (uncovered) and 0 volts (covered).

## c. Adjustment.

(1) Loosen the four pressure screws (fig. 416 ) on the read station mounting block.


Figure 4-14. Metering capstan pressure requirement.


Figure 4-15. Picker solenoid requirement.
(2) While monitoring the photoamplifier inputs (ROWI through ROW12, BCP, and ECP-fig. 814), carefully rotate the phototransistor as follows. Insert a piece of plastic or plastic tipped screwdriver ffig. 4-16) between the pins on the phototransistor and carefully turn the phototransistor until the photocell output indicated on the oscilloscope is at least +4.3 volts dc (uncovered) and at least +3.3 volts (covered). Assure the phototransistors are bottomed in the sockets and take care not to break the pins on the phototransistors. If the phototransistors do not switch voltages between the covered and uncovered conditions, go to step (4) below.
(3) Tighten the pressure screws (fig. 4-16) on the read station mounting block to secure the phototransistors.
(4) If the monitored voltage is approximately 3.3 vdc and does not change when the phototransistors are adjusted, check the position of the read station mounting block. While monitoring the photoamplifier inputs (fig. 8-14), adjust the position of the read station mounting block until the voltage changes from +3.3 vdc to +4.3 vdc. Secure the read station mounting block and repeat the check of all 14 inverter outputs noted in b(3) above.
d. Bench Adjustment Procedure. The procedure outlined in b and c above is preferred for checking read station phototransistor operation since it also checks printed circuit card A1A6 circuitry. Figure 4-16. however, outlines test equipment connections for bench operation and adjustment. With the test equipment connections as illustrated in figure 4-16, a 1 -volt indication on the VTM is equivalent to 1 ma of current from the phototransistors. With the reader lamps illuminated and no card in the reader head, the VTVM should indicate an optimum value of 6 volts ( 6 ma ). Any value between 2 volts ( 2 ma .) and 10 volts ( 10 ma .) should normally provide satisfactory operation.

## 4-58. Adjustment of Hopper Empty Lamp

fig. 4-17)
a. Requirement. The hopper empty lamp must be positioned so that proper response is obtained from the hopper empty phototransistor.
b. Method Checking.
(1) Set the oscilloscope input voltage selector to the 1 -volt position and connect the input probe to pin D of PC card A1A6 in the logic assembly.
(2) Turn on the card reader. Insure that no cards are in the hopper and all lamps of the light station are lighted.
(3) Check indication. Voltage level should be between 4.3 and 4.4 volts dc.
(1) Loosen mounting screws securing the hopper-empty lampholder (fig. 4-17).
(2) While monitoring voltage on pin $D$ of A1A6, adjust position of the lampholder for a 4.3 to 4.4 volt dc indication. Note that monitored voltage will be approximately 3.3 volts, until lampholder is correctly positioned.

## NOTE

## Correct voltage must be obtained without moving lampholder past the input card guide into the card path.

(3) Secure the mounting screws and recheck for 4.3 to 4.4 volts dc.
d. Bench Adjustment Procedure. Figure 4-17 outlines test equipment connections to enable check to be performed on the bench. With test equipment connections as illustrated in figure 4-17, a 1 -volt indication on the VTVM is equivalent to 1 ma . of current from the phototransistor. Adjust the position of the light station assembly for a nominal indication of 6 volts ( 6 ma.). Any value between 2 volts ( 2 ma .) and 10 volts (10 ma.) should normally provide satisfactory operation.

## 4-59. Adjustment of Reluctance Pickup-Timing Gear Gap fig. 4-18)

a. Requirement. The gap between the polepiece of reluctance pickup PU1 and the timing gear teeth must be such that the pickup provides 5.8 volts peak-to-peak nominal ( 5.5 to 6.5 volts) with a load impedance of 1,000-ohm operating at 120 volts 60 Hz , and 4.8 volts peak-to-peak nominal ( 4.5 to 5.5 volts) operating at 50 Hz .
b. Method of Checking. Connect a $1,000-\mathrm{ohm} 1 / 4-$ watt loading resistor and an oscilloscope across the terminals of the reluctance pickup. Disconnect connector plug P1 from jack J3 to remove the reluctance pickup output from remaining circuitry. The waveform on the oscilloscope should be a 2.5 -kilohertz sine wave with amplitudes as in a above. The amplitude varies as the gap between the reluctance pickup and the timing gear changes due to gear rotation.

## c. Adjustment.

CAUTION
Remove all power from the card reader before adjusting the reluctance pickup. Do not apply power until the jam nut has been tightened.
c. Adjustment.
(1) Loosen the three mounting screws so that the reluctance pickup bracket can be moved.
(2) Position the bracket so that the reluctance pickup is visually alined radially with the timing gear and tighten the three mounting screws.
(3) Place a 0.003 -inch feeler gage between the reluctance pickup polepiece and the timing gear teeth. Rotate the timing gear to the point where the clearance between the polepiece and the timing gear teeth is least.

## CAUTION

Rotate the timing gear manually at least one full turn to insure the pole piece does not scrape the gear teeth at any point on the gear.
(4) Loosen the jamnut and rotate the entire reluctance pickup in the threaded mounting hole until the gap between the polepiece and the timing gear teeth
is 0.003 inch (the 0.003 -inch feeler gage can just be withdrawn.

## CAUTION

Do not tighten the jamnut to more than 16 inch-pounds.
(5) Tighten the jamnut to 16 inch-pounds of torque and recheck the gap with the 0.003 -inch feeler gage.
(6) Recheck the reluctance pickup output as in b above. If the voltage is below that required in a above, remove all power from the card reader and decrease the gap between the polepiece and the timing gear teeth, in 0.0005inch increments, until the correct voltage is obtained. If the voltage is above 6.5 volts peak-to-peak, remove power from the card reader and increase the gap between the polepiece and the timing gear teeth, in 0.0005 -inch increments, until the correct voltage is obtained.


| Card Row | PC Card A1A6 Pins |  |  |
| :---: | :---: | :---: | :---: |
|  | Photo Amplifier | Inverter |  |
|  | In | Out | Out |
| 12 | L | K | M |
| 11 | 5 | C | E |
| 0 | 4 | H | F |
| 1 | AA | Z | X |
| 2 | 21 | I | W |
| 3 | 19 | - | 20 |
| 4 | 18 | J | 22 |
| 5 | 17 | - | 16 |
| 6 | 14 | 6 | $\nabla$ |
| 7 | 13 | - | 11 |
| 8 | 12 | 7 | N |
| 9 | 10 | 9 | 8 |
| Hop Emp | D | 2 | - |
| BOC | S | T | O |
| EOC | 15 | R | P |

TM7440-215-15-48-C4
Figure 4-16. Read station, phototransistor requirement.


TM7440-215-15-49-C4
Figure 4-17. Hopper empty lamp requirement.


Figure 4-18. Reluctance pickup requirement.

## 4-60. Adjustment of Offset Idler

(fig. 4-19)
a. Requirement. When the offset solenoid is not energized, the offset idler must be parallel to the offset capstan, thus transporting the processed cards to the stacker elevator in a straight line. When the solenoid is energized, the card must be offset $1 / 4$ to $3 / 4$ inch in the stacker elevator so that the card can be readily identified visually.
b. Method of Checking. If power is applied to the card reader, the adjustment is checked by observing whether cards form a straight stack in the elevator, with the deck stacked against the rear surface of the elevator. Offset cards should project approximately $1 / 4$ to $3 / 4$ inch from the stacker. With no power applied. to the reader, the adjustment can be checked by turning the drive shaft manually to transport a card into the stacker. The card should leave the offset capstan in a straight line perpendicular to the roller shafts when the solenoid is not actuated. When the solenoid is actuated, the card should be offset.
c. Adjustment.
(1) Adjust the idler stop screw so that the cards are transported to the stacker elevator in a straight line when the offset solenoid is not energized. Turn the screw counterclockwise to move cards toward the panel, or clockwise to move cards away from the panel.
(2) Manually actuate the solenoid and adjust the offset stop screw to obtain proper offsetting. Turn the screw counterclockwise to increase the projection of
offset cards, and turn it clockwise to decrease the projection.

## 4-61. Adjustment of Offset Solenoid

 fig. 4-19)a. Requirement. The offset solenoid plunger must have sufficient travel to allow full motion of the idler yoke and still operate consistently with the available voltage. The offset solenoid plunger must not reach bottom when fully actuated.
b. Method of Checking.
(1) With power to the card reader off, disconnect the plug at connector J2.
(2) Connect a variable dc power supply to pins E (negative) and F (positive) of connector J2.
(3) Increase the voltage of the dc power supply until the solenoid pulls in. Nominal pull-in voltage is 37 volts ( 35 to 40 volts).
(4) Alternate method of checking can be accomplished by removing front cover from the card reader, and with power off, disconnect plug P1 located on the front panel next to offset assembly A3. Connect a variable dc power supply to P 1 as follows: negative to lower pin 1, and positive to upper pin 2. Perform (3) above.
c. Adjustment. Loosen the solenoid bracket mounting screws, and move the solenoid toward the offset idler if more than 37 volts is required to actuate the solenoid, or move the solenoid away from the offset idler if less than 37 volts is required to actuate the solenoid.

## 4-62. Adjustment of Card Guides

## (fig. 4-20)

a. Requirement. The card guides must be positioned so that the cards move without jamming up or becoming damaged.
b. Method of Checking. Visually check that the lower card guide is either flush or not more than 0.005 inch below the lower surface of the gap where the cards come out of the picker and read assembly and that the upper card guide is above the upper surface of the gap.
c. Adjustment. Loosen the two mounting screws and position the lower card guide so that it is either flush or not more than 0.005 inch below the lower surface of the gap where the cards come out of the picker and read assembly. Hold the lower card guide in this position and move the upper card guide as high as possible. Tighten the two mounting screws.

## 4-63. Adjustment of Stacker Spring Tension

 fig. 4-21)a. Requirement. The stacker elevator must rest at the upper limit under a pressure of 5 ounces nominal (4 to 10 ounces or, 113 to 283 grams) when the stacker elevator is empty and must be depressed proportionately as cards enter the stacker.
b. Method Checking.
(1) Press down on the stacker elevator platform using a push-type spring scale, then slowly release the pressure. The stacker elevator should rise to the upper limit under a pressure of 5 ounces nominal ( 4 to 10 ounces) ( 113 to 283 grams).
(2) During the normal card processing operation of the card reader, observe that the stacker
elevator is depressed proportionately as cards enter the stacker.
c. Adjustment. Loosen the spring hanger setscrew and move the spring hanger up or down to obtain the requirement in $a$ above.

## 4-64. Adjustment of Elevator Stop

## (fig. 4-21)

a. Requirement. The top limit of stacker elevator travel should be at a point where the top of the stacker elevator is $1 / 4$ inch below the slot in the panel.
b. Method of Checking. With the stacker elevator empty, measure the distance between the top of the stacker elevator and the top of the panel slot.
c. Adjustment. Loosen the setscrew on the


Figure 4-19. Offset idler requirement.
elevator stop and move the stop up or down on the elevator shaft.

## 4-65. Adjustment of Stacker Full Sensor

(fig. 4-21)
a. Requirement. When the stacker elevator contains 1,000 or more cards, switch S1 must be actuated to provide a contact closure across pins $f$ and $g$ of connector J1. Contacts must be open when there are less than 1,000 cards in the stacker elevator.
b. Method of Checking. Use an ohmmeter to check for an open circuit across pins $f$ and $g$ of connector J1 with no cards in the stacker elevator. Place 1,000 cards in the stacker elevator and check to see that the open circuit still exists. As 50 additional cards are placed in the stacker elevator, the ohmmeter should indicate continuity.


Figure 4-20. Card guide requirement.
c. Adjustment. Loosen the two attaching screws on the switch and position the switch to obtain the required response.

## 4-66. Adjustment of Card Input Support (fig. 4-22)

a. Requirement. The card input support must be positioned so that the lower end, adjacent to the picker frame, is one card length ( $73 / 8$ inches) plus $0.02-0.01$ inch from the face of the picker throat block.
b. Method of Checking.
(1) Place a standard punched card in position on the picker frame and push it snugly against the picker throat block.
(2) Use a feeler gage to measure the distance between the end of the punched card and the card input support.
c. Adjustment. Loosen the mounting screws on the rear of the panel, and move the support until the proper distance is obtained.

## 4-67. Adjustment of Power Supply Output Voltages

a. Requirement. The adjustment of the power supply output voltages is an electrical adjustment which is made by means of four potentiometers to produce the specified dc output voltages at specific test points within the power supply. These adjustments are made with the power supply connected into the card reader and power on.
b. Method of Checking. Connect a digital voltmeter to the following test points at the front panel of the power supply. The dc voltages measured should fall within the tolerances specified.

| Test points | Voltages (dc) |
| :---: | :---: |
| +4.75 and COM | $4.75 \pm 0.05$ |
| -12V and COM | $-12.00 \pm 0.06$ |
| + 12V and COM | $+12.00 \pm 0.06$ |
| -48V and COM | $48.00 \pm 0.24$ |

c. Adjustment. If any of the voltages specified in b above are out of tolerance, the corresponding potentiometer should be adjusted to bring the voltage into tolerance. The potentiometers are listed as follows:

| DC voltage | Potentiometer to be adjusted | Fig. 4-4 <br> item <br> number |  |
| :---: | :---: | :---: | :---: |
|  |  |  | 92 |
| +475 | R24 | (on assy PS1A1) | 92 |
| +12 | R17 | (on assy PS1A2) | 93 |
| -12 | R32 | (on assy PS1A2) | 93 |
| -48 | R18 | (on assy PS1A3) | 94 |

## 4-68. Adjustment of Power Supply Regulated Supply

a. Requirement. After the power supply output voltage adjustments are performed, the performance of the regulated supply located on sequence module PS1A12 in the power supply should be checked.
b. Method of Checking. Connect a digital voltmeter between the test points TP11 (+) and TP13 (common) located on sequence module PS1A12 in the power supply (40, fig. 4-4). The power supply should be operating in the normal manner in the card reader, with normal system power turned on. The voltage measured should be $+15.0 \pm 0.1$ volt dc.


Figure 4-21. Stacker spring, elevator stop, and stacker full sensor requirements.
When taking voltage measurements
on power supply PS1 sequence
module A12, use insulated test
connectors to avoid possible short
circuits between test points and
copper runs.
c. Adjustment. If the voltage from test point TP11 to TP13 is not within tolerance, adjust potentiometer R73 on sequence module A12 (40, fig. 4-4).

4-69. Adjustment of Power Supply Overvoltage Limit
a. Requirement. After the +4.75 output voltage has been checked and adjusted (para 4-67), the overvoltage limit circuit for the +4.75 -volt output should be checked to make certain that the trip point of 5.5 volts dc is not exceeded.
b. Method of Checking.
(1) Disconnect the wire connection from PS1TB2, pin 2.
(2) Connect a digital voltmeter, Digitec 251-1, or equivalent, to the test point labeled $+4.75(+)$ on the power supply front panel and the COM test point.
(3) Slowly adjust potentiometer PSA1R24 to obtain an increase in the +4.75 -volt output, while observing the digital voltmeter. Continue to increase the voltage while observing the voltmeter until the meter indication suddenly drops to zero volts. The maximum voltmeter indication (occurs immediately before voltage drops to zero) is termed the trip point and should be 5.40 volts $\mathrm{dc} \pm 0.05$. If the trip point voltage is out of tolerance, adjust potentiometer PS1A1R30 (92, fig. 44). Repeat the check and adjustment until the trip point voltage is within the specified tolerances.
(4) Adjust PS1A1R24 to meet the requirements of paragraph 4-67.
(5) Disconnect the digital voltmeter.
(6) Reconnect the wire connection to PS1 TB2, pin 2.

## 4-70. Adjustment of Vacuum Relief Valve

NOTE
The following adjustment requires two people.
a. Requirement. The picker requires a vacuum of 5 to 7 inches Hg . while picking a card. This value is obtained when the relief valve fig. 4-23) is properly adjusted.
b) Method of Checking. With the card reader motor operating, place a card in the hopper and hold the card against the picker belts to close the perforations in the belts. Manually actuate the picker solenoid and check the vacuum indicated by the gauge (fig. 4-23) on the pump assembly.
c. Method of Adjustment. Loosen locknut on relief valve assembly. With motor operating, hold a card in the hopper against the picker belts and actuate the picker solenoid as in b above. Turn adjustment nut until the gauge indicates a minimum value of 5 inches Hg . Clockwise rotation of the adjustment nut increases the vacuum and counter,-clockwise rotation decreases the


Figure 4-22. Card input support requirement.


TM 74 40-215-15-C1-2
Figure 4-23. Vacuum relief valve requirements.


Figure 4-24. Card path clearance adjustment.

## 4-71. Adjustment of Card Path Clearance (fig. 4-24)

a. Requirement. There should be sufficient clearance between the light station assembly and the angle bracket assembly (phototransistor mounting bracket) to allow free card movement through the read station.
b. Method of Checking. Insert a standard unpunched data card between light station assembly and angle bracket assembly from the front of the machine, immediately to the left of the outboard capstan and outboard idler. Withdraw it
moderately fast. There should be no significant drag on the card, indicating that there is sufficient clearance for free card movement.
c. Method of Adjustment. Add a minimum thickness of shims between light station assembly and light station platform, to eliminate any significant drag on a card as in b, above. An equal thickness of shims should be installed around each of the two light station assembly mounting screws. To insure proper alignment with phototransistors, the light station assembly should be held to the left while tightening the mounting screws.

## CHAPTER 5

PRINTED CIRCUIT CARD MAINTENANCE INSTRUCTIONS

## Section I. GENERAL

## 5-1. Scope of PC Card Maintenance

a. This chapter includes instructions for performing corrective maintenance procedures on PC cards. Isolation of a malfunction in the card reader to a PC card is given in chapter 4. The instructions in this chapter are used to isolate the malfunction to a defective part in the PC card and to replace the defective part.
b. PC card maintenance includes-
(1) Testing a PC card suspected to be defective.
(2) Troubleshooting using manual techniques.
(3) Replacement of defective parts.
(appx C) for a list of the tools and test equipment required for maintenance of the printed circuit cards of the card reader.

## 5-2. Tools and Test Equipment Required

## Refer to the maintenance allocation chart

## Section II. TROUBLESHOOTING PRINTED CIRCUIT CARDS

## 5-3. Testing Procedure

If a PC card is suspected to be defective, install it in a card reader which is known to be operable. Then operate the card reader with an associated CCU and output device to read out the information content on punched cards containing all possible characters (fig. 3-4). If cards are picked and fed, and all characters are properly read out, the PC card being checked is considered good. If a malfunction occurs, locate and correct the fault as described in paragraphs 5-4 through 5-25.

## 5-4. General Troubleshooting Procedure

The first step in servicing a defective PC card is to perform a visual inspection. If this does not help in localizing the fault, signal tracing and signal substitution techniques are required.

## 5-5. Visual Inspection

Carefully inspect the PC card for evidence of overheating. Check for corrosion, or loose connections.

## 5-6. Signal Tracing

a. Place the PC card on an extender board and, with power off, install it in an otherwise operable card reader. Operate the card reader to simulate the
condition under which tile malfunction was observed. Then use standard signal tracing techniques to isolate the defective part. A thorough knowledge of the operation of the card reader circuits as given in chapter 3 is required to effectively use signal tracing techniques.
b. The voltages and waveforms at most test points may be observed with the oscilloscope. In general, signals at input and outputs of integrated circuit logic element modules switch between +4.5 volts dc (high) and 0 volt dc (low). Determine whether the voltage at a specific terminal is high or low at any time by studying the operating conditions at that time. For voltages at inputs and outputs of discrete circuit logic elements, refer to paragraph 3-25.
c. Refer to paragraph 5-9 for the location of parts on PC cards. Refer to figure 5- for the location of terminals on integrated circuit logic element modules. Figure 5-1 applies to all types of integrated circuit logic elements.
d. The card reader can be operated to read only one card at a time using the SINGLE FEED switch on the control panel. Each time this switch is pressed, a single card is picked and read; however, the card reader cannot normally be made to read one character at a time. If the PC card being checked contains

TERMINLLL 6-+4.5VOC
TERMINAL I-OV OC


TM7440-215-15-60
Figure 5-1. Location of terminal. on integrated circuit modules.
circuits which process the character data bits, repetitive -waveforms for signal tracing can be obtained
by using a punched card with the identical character punched in each of the 80 columns.
e. Each lamp driver microcircuit module contains three independent lamp driver circuits. Figure 5-1.1 shows the location and numbering of terminals on the microcircuit module.

## 5-7. Signal Substitution

In some cases, the effort of isolating a malfunction within a complex logic circuit can be simplified by using signal substitution techniques. Specifically, any point or points at, the input to ,a logic element may be grounded, thereby making the operation of the logic element easily predictable. This method cannot normally be used to insert a high level ( +4.5 volts) without physically disconnecting the signal input from the logic element; therefore, it is not recommended to use signal substitution for high level inputs.

## Section III. REPAIR OF PRINTED CIRCUIT CARDS

## 5-8. General Parts Replacement Techniques

Most of the parts on at PC card can be replaced easily without special procedure. For PC card soldering techniques, refer to TB SIG 222 (Army), TO 0025-234 (Air Force), or NW 00-15PA-1 (Navy) (app. A). When replacing integrated circuit logic elements, it is important to unsolder only one termi-
nal at a time, using a solder syringe to remove the solder before unsoldering the next terminal.

## 5-9. Parts Location

Tile locations of all replaceable parts on the PC cards of the card reader are shown ir figures 5-2 through 5-23.

| TERMINAL | FUNCTION | TERMINAL | FUNCTION |
| :---: | :---: | :---: | :---: |
| 1 | OUTPUT I | 6 | INPUT 3 |
| 2 | InPUT 1 | 7 | +12 VOLTS DC |
| 3 | OUTPUT 2 | 8 | - 12 VOLTS OC |
| 4 | INPUT 2 | 9 | LAMP TEST |
| 5 | OUTPUT 3 | 10 | GROUND |



TM7440-215-15-Cl-3-1
Figure 5-1.1. Location of terminals of microcircuit lamp driver modules.

## 5-10. Test Data Charts

a. The test data charts contained in this section may be used when troubleshooting printed circuit cards to determine the type of signal which should be present under certain conditions. This should prove as an aid in localizing a malfunction to a particular circuit on the suspected defective card.
b. For all cards installed in logic assembly A1, ground is available on pin 1 or A of the printed circuit card connector. Pin 2 of B of each PC card connector supplied +4.5 volts to the printed circuit cards. By using a short lead terminated at both ends with alligator clips, these pins can be used as a source of ground ( 0 volts) or active ( +4.5 volts) signals for troubleshooting the printed circuit cards.
c. Test data charts are arranged to show the point of test (Test point column) to which the meter, oscilloscope, or other test equipment is connected; the conditions under which the measurement should be made (Test conditions column); and the results which should be obtained if the circuit being tested is good (Normal indication column). It should be noted that the Normal indication column gives the expected results for normally operating equipment.
d. Unless otherwise specified, all test data in the charts assume the printed circuit board connected to an otherwise operable equipment, with the equipment operating as part of a terminal configuration.

## 5-11. Test Card Deck

a. Prepare a deck of test cards (at least 100) punched with 16 asterisks followed by the 64 .

ASCII characters listed in figure 3-4. The sequence of characters on the card should be shown in Table 5-1. These test cards will be used to provide appropriate input signals to the card reader during certain test conditions specified in the test data charts (para 5-12 through 5-26).

Table 5-1. Test Pattern Character Sequence

| Card column | Character | Punched code |
| :---: | :--- | :---: |
| 1 | *Asterisk | $11,8,4$ |
| 2 | $" "$ | $"$ |
| 3 | $"$ | $"$ |
| 4 | $"$ | $"$ |
| 5 | $"$ | $"$ |
| 6 | $"$ | $"$ |
| 7 | $"$ | $"$ |
| 8 | $"$ | $"$ |
| 9 | $"$ | $"$ |
| 10 | $"$ | $"$ |

Table 5-1.Continued

| Card column | Character | Punched code |
| :---: | :--- | :---: |
| 16 | * Asterisk | 11, 8, 4 |
| 17 | Space | No Punches |

18 ! Exclamation Point
No Punches
12,8,7
"Quotation Mark
\# Number sign 7,8
\# Number sign
\$ Dollar Sign
8,3
\% Percent
11,8,3
\& Ampersand
10,4,8
' Apostrophe
( Opening Parenthesis
' Closing Parenthesis
12
( Opening Parenthesis
) Closing Parenthesis

* Asterisk
12,8,5
11,8,5
11,4,8
+ Plus
12,8,6
, Comma
10,3,8

| - Hyphen | 11 |
| :--- | ---: |
| - Period | $12,3,8$ |


| / Slant | 10,1 |
| :--- | ---: |
| 0 Zaro | 10 |


| 0 Zero | 10 |
| :---: | ---: |
| 1 | 1 |
| 2 | 1 |

2
3
4
5
5


| 7 |  |
| :--- | :--- |
| 8 |  |


| 8 |  |
| :--- | :--- | :--- |
| 9 |  |
| . |  |

; Colon
8,2
11,6,8
12,4,8
8,6
10,8,6
10,8,7
8,4
12,1
12,2
12,3
12,4
12,5
12,6
12,7
12,8
12,9
11,1
11,2
11,3
11,4
11,5
11,6
11,7
11,8
11,9
10,2
10,3
10,4
10, 5
10, 6

Change 6 5-2.1

TM 11-7440-2 15-15/NAVSHIPS 0967-324-002D/TO 31 W4-2G-3 1
Table 5-1.Continued

| Card column | Character | Punched code |
| :---: | :---: | :---: |
| 73 | X | 10,7 |
| 74 | Y | 10,8 |
| 75 | Z | 10,9 |
| 76 | O- Plus zero | 12,10 |

5-12. PC Card A1A1 (A65209-002) Test Data Chart
(Fig. 5-12 and 8-10

| Test points | Test conditions | Normal indications |
| :---: | :---: | :---: |
| Typical SOL DR (B) or SOL DR (C) output (XA1-5 or XA1-6). XA1-14 | PC card A15 removed from logic assembly A1 (fia. 4-2), power on, and: <br> a. +4.5 volts dc applied to input (XA1-D) - <br> b. ground applied to input (XA1-D) Initial power turn-on. | a. -48 volts dc. b. 0 volts dc. +4.5 volts dc pulse, 330 msec wide, with slow decay |

## 5-13. PC Card A1A3 (SM546659-001) Test Data Chart

(Fig. 5-14) and 8-11)

| Test points | Test conditions | Normal indic ations |
| :---: | :---: | :---: |
| Typical lamp driver output (ХАЗ-U). | PC card A15 removed from logic assembly A1 (fig. 4-2), power on, and: <br> a. LAMP TEST switch A3Z3 pressed . <br> b. +4.5 volts dc applied to input (XA3-17). <br> c. ground applied to input (XA3-17) | a. 0 volts dc. b. 0 volts dc. c. 15 volts ac. |

## 5-14. PC Card A1A4 (A65215-001) Test Data Chart

Fig. 5-13 and 8-12)

| Test points Test conditions |  | Normal indications |
| :---: | :---: | :---: |
| RCVR-1C output (XA4-D) | Jack J1 removed from logic assembly A1 (fig. 4-2), power on, and: <br> a. +6.2 volts dc applied to input (XA4-E) <br> b. -6.2 volts dc applied to input (XA4-E) | a. +4.5 volts dc. <br> b. 0 volts de. <br> a. +4.5 volts dc. <br> b. 0 volts dc. |
| Typical RCVR-1A or RCVR-1B output (XA4-8). | Jack J 1 removed from logic assembly Al fig. 4-2), power on, and: <br> a. ground applied to input (XA4-9) <br> b. open applied to input (XA4-9) |  |
| XMTR-1B output (XA4-21) | PC card A16 removed from logic assembly A1 (fig. 4-2), power on, and: <br> a. ground applied to both inputs (XA4-22 and XA423). | a. Open circuit (+6.2 volts dc may be reflected from associated receiver circuit in the CCU). <br> b. Open circuit (+6.2 volts may be reflected from associated receiver circuit in the CCU). <br> c. 0 volts dc. |
|  | b. ground applied to input (XA4-22) and +4.5 volts dc applied to input (XA4-23). |  |
|  | c. +4.5 volts dc applied to both inputs (XA4-22 and XA4-23). |  |
| Typical XMTR-1A output (XA4-14). | PC card A16 removed from logic assembly AI (fig. 4-2), power on, and: <br> a. +4.5 volts dc applied to input (XA4-16) <br> b. ground applied to input (XA4-16) | a. 0 volts dc. <br> b. Open circuit ( 6.2 volts dc may be reflected from associated receiver circuit in the CCU). |

Change 6 5-2.2

## 5-15. PC Card A1A5 (A65205-001) Test Data Chart

(Fig. 5-11 and 8-13)

| Test points | Test conditions | Normal indications |
| :---: | :---: | :---: |
| Typical XMTR-2 output (XA5-U). | PC cards A4 and A13 removed from logic assembly <br> A1 fig. 4-2), power on, and: <br> a. ground applied to input (XA5-10) <br> b. +4.5 volts dc applied to gate input (XA5-10) and: <br> (1) +4.5 volts dc applied to input (XA5-W) <br> (2) ground applied to input (XA5-WV) | a. -6.2 volts dc. b. (Output enabled) (1) +6.2 volts dc. <br> (2) -6.2 volts dc |

5-16. PC Card A1A6 (A52630-001) Test Data Chart
(Fig. 5-3 and 8-14

| Test points | Test conditions | Normal indications |
| :---: | :---: | :---: |
| Typical PHOTO AMPL-1 <br> output (XA6-X). <br> XA6-23 | Power on, hopper loaded with blank (unpunched cards), and SINGLE FEED switch A3Z4 pressed. <br> a. Photocells not covered by card <br> b. Photocells covered by card <br> Power on, hopper loaded with blank (unpunched cards), and SINGLE FEED switch A3Z4 pressed. <br> a. Photocells not covered by card <br> b. Photocells covered by card | a. +4.5 volts dc. b. 0 volts dc. <br> a. +4.5 volts dc. <br> b. 0 volts dc. |

## 5-17. PC Card A1A7 (A65145-001) Test Data Chart

(Fig. 5-8 and 8-15

| Test points | Test conditions | Normal indications |
| :---: | :---: | :---: |
| Typical Data Register latch output (XA7-16). | PC cards A14 and A16 removed from logic assembly A1 fig. 4-2), power on, and: <br> a. ground applied to inputs (XA7-X, XA7-Y, and XA7-U) and +4.5 volts de applied to input (XA7T). <br> b. ground applied to inputs (XA7-X, XA7-U, and XA7-T) and +4.5 volts dc applied to inputs (XA7-Y and XA7-N). | a. 0 volts dc. <br> b. +4.5 volts dc. |

## 5-18. PC Card A1A8 (A52634-001) Test Data Chart

(Fig. 5-4 and 8-16

| Test points Test conditions |  | Normal indications |
| :---: | :---: | :---: |
| XA8-C | Power on with test deck (para 5-11) loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed | a. 0 volts dc. <br> b. 0 volts dc. <br> a. 0 volts dc. <br> b. 0 volts dc. <br> a. 0 volts dc. <br> b. Train of 0 to +4.5 volt dc pulses. <br> a. 0 volts dc. <br> b. 0 volts dc. |
| XA8-D | Power on with test deck (para 5-11) loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed |  |
| XA8-U | Power on with test desk para 5-11) loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed |  |
| XA8-4 | Power on with test deck (para 5-11) loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed |  |

## 5-18. PC Card A1 A8 (A52634-001) Test Data Chart (cont.)

| Test points |  |
| :--- | :--- |
| XA8-6 | Test conditions |
| Power on with test deck (para 5-11) loaded in hopper and: |  |
| a. MASTER RESET switch A1S1 pressed |  |
| b. LOCAL TEST switch A3Z5 pressed |  |$\quad$| a.a volts dc. <br> b. Two 0 to +4.5 volt dc pulses per <br> card (columns 76 and 78). |
| :--- |

## 5-19. PC Card A1A9 (A53725-001) Test Data Chart

(Fig. 5-6 and 8-17

| Test points | Test conditions | Normal indications |
| :--- | :--- | :--- |
| Typical decode gate (Z4B) out- <br> put (XA9-C) | Power on with test deck(para 5-11) loaded in hopper <br> and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed | a. 0 volts dc. <br> b. One 0 to +4.5 volt dc pulse <br> per card (column 40). |

## 5-20. PC Cards A1A10, A1A11, and A1A12



## WARNING

Do not remove PC Card AIA12 prior to removing AC voltage to Punched Card Card Reader from the AC power sources.

5-21. PC Card A1A13 (A52622-001) Test Data Chart
(Fig. 5-2 and 8-21)

| Test points |  | Test conditions |
| :--- | :--- | :--- |
| XA13-Z | Power on with test deck (bara. 5-11) loaded in hopper <br> and: |  |
|  | a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed | a. +4.5 volts dc. <br> b. Train of +4.5 to volt dc pulses. |

## 5-21. PC Card A1A13 (A526622-001) Test Data Chart (cont.)

| Test points | Test conditions | Normal indications |
| :---: | :---: | :---: |
| XA13-4 | Power on with test deck (para 5-11) loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed | a. +4.5 volts dc. <br> b. Train of +4.5 to 0 volt dc pulses. |
| XA13-20 | Power on with test deck (para 5-11) loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed | a. +4.5 volts dc. <br> b. Train of +4.5 to 0 volt dc pulses. |
| XA13-22 | Power on with test deck (para 5-11) loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A2Z5 pressed | a. +4.5 volts dc. <br> b. Train of +4.5 to 0 volt dc pulses. |
| XA13-23 | Power on with test deck (para 5-11) loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed | a. 0 volts dc. <br> b. Train of 0 to +4.5 volt dc pulses. |

5-22. PC Card A1A14 (A65175-001) Test Data Chart
(Fig. 5-9 and 8-22

| Test points Test conditions |  | Normal indications |
| :---: | :---: | :---: |
| XA14-6 | Power on and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed with hopper loaded with test deck (para 5-11). <br> c. LOCAL TEST switch A3Z5 pressed with hopper loaded with blank (unpunched) cards. | a. +4.5 volts dc. <br> b. Train of +4.5 to 0 volt dc pulses. <br> c. +4.5 volts dc. |
| XA14-7 | Power on with test deck (para 5-11) loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed | a. 0 volts dc. <br> b. Train of 0 to +4.5 volt dc pulses. |
| XA14-9 | Power on with test deck para 5-11) loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed (column 17). | a. 0 volts dc. <br> b. One 0 to +4.5 volt dc pulse per card |
| XA14-14 | Power on with test deck para 5-11 loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed | a. 0 volts dc. <br> b. Train of 0 to +4.5 volt dc pulses. |
| XA14-18 | Power on with test deck (para 5-11) loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z5 pressed | a. 0 volts dc. <br> b. Train of 0 to +4.5 volt dc pulses. |

## 5-23. PC Card A1A15 (A65153-001) Test Data Chart

(Fig. 5-10 an 8-23)

| Test points | Test conditions | Normal indications |
| :---: | :---: | :---: |
| XA15-J and XA15-V | Power on with hopper loaded with a deck of cards that includes one card creased so that it will cause a pick fail, and LOCAL TEST switch A3Z5 pressed <br> a. Observe XA15-V on good cards <br> b. Observe XA15-V on pick fail <br> c. Observe XA15-J on pick fail | a. 0 volts dc. <br> b. 0 to +4.5 volt dc pulse after a delay. <br> c. $-4.5-$ volt dc level after a delay. |

Change 2 5-2.5

## 5-23. PC Card A1A15 (A65153-001) Test Data Card (cont.)

| Test points $\quad$ Test conditions |  | Normal indications |
| :---: | :---: | :---: |
| XA15-K <br> XA15-L | Power on <br> Power on and: <br> a. MASTER RESET switch A1S1 pressed <br> b. PC card A16 removed from logic assembly A1 (fig. 4-2) and -+4.5 volts dc applied to input (XA15-U). | +4.5 volt dc pulses. <br> +4.5 volts dc. <br> b. One +4.5 to 0 volt dc pulse when +4.5 volts dc was applied to input (XA15-U). |
| XA15-6 | Power on and: <br> a. MASTER RESET switch A1S1 pressed <br> b. PC card A14 removed from logic assembly A1 (fig. 4-2) and then: <br> (1) +4.5 volts dc applied to input (XA15-7) <br> (2) open applied to input (XA15-7) | a. 0 volts dc. <br> b. Observe following: <br> (1) 0 volts dc. <br> (2) 0 to +4.5 volt dc pulse after a delay. |

5-24. PC Card A1A16 (A65141-001) Test Data Chart
(Fig. 5-7 and 8-24)

| Test points Test conditions |  | Normal indications |
| :---: | :---: | :---: |
| XA16-P | Power on with a deck of cards loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. START switch A3Z7 pressed | a. 0 volts dc. <br> b. +4.5 volts dc. |
| XA16-6 | Power on and: <br> a. MASTER RESET switch A1S1 pressed and held <br> b. MASTER RESET switch A1S1 released | a. +4.5 volts dc. <br> b. 0 volts dc. |
| XA16-13 | Power on with cards loaded in hopper and: <br> a. MASTER RESET switch A1S1 pressed <br> b. SINGLE FEED switch A3Z4 pressed | a. 0 volts dc. <br> b. One 0 to +4.5 volt dc pulse. |
| XA16-14 | Power on with cards loaded in hopper and: <br> a. STOP switch A3Z6 pressed <br> b. LOCAL TEST switch A3Z5 pressed | a. 14.5 volts dc. <br> b. 0 volts dc until hopper is empty. |
| XA16-18 | Power on, assigned, and AUDIBLE RESET switch A3Z1 pressed. | 0 to +4.5 volt de pulse when switch is first pressed. |
| XA16-21 | Power on with cards loaded in hopper and SINGLE FEED switch A3Z4 pressed. | 0 to +4.5 volt de pulse while card is being processed. |

5-25. Power Supply PS1 Test Data Chart
(Fig. 4-4 and 8-7).

## CAUTION

When taking voltage measure on power supply PS1 sequence module A12, use insulated test connectors to avoid possible short circuits between test points and copper runs.

| Test points | Test conditions | Normal indications |
| :--- | :--- | :--- |
| PS1TP2 to PS1TP1 (Common) | Power on | $+4.75 \mathrm{vdc} \pm 1 \%$ |
| PS1TP3 to PSTP1 | Power on |  |
| PS1TP4 to PS1TP1 | Power on |  |
| PS1TP5 to PS1TP1 | Power on |  |
| PS1A12TP3 to TP13 | Power on | $-42.0 \mathrm{vdc} \pm 1 \%$ |
| PS1A12TP4 to TP13 | Power on | $-12.0 \mathrm{vdc} \pm 1 \%$ |
| PS1A12TP6 to TP13 | Power on | $+12.0 \mathrm{vdc} \pm 1 \%$ |
| PS1A12TP9 to TP13 | Power on | $+4.75 \mathrm{vdc} \pm 1 \%$ |
| PS1A12TP1 to TP13 |  | $+48.0 \mathrm{vdc} \pm 1 \%$ |





I

Figure 5-2. PC card A13 (No. A52622-001). component location diagram.


Figure 5-3. PC card A6 (No. A52630-001), component location diagram.


Figure 5-4. PC card A8 (No. A52634-001), component location diagram.


Figure 5-5. PC cards ,A10 and A12 (No. 53721-001), component location diagram.


Figure 5-6. PC cards A9 and A11 (No. A53725-001), component location diagram.


Figure 5-7. PC card A16 (No. A65141-001), component location diagram.


Figure 5-8. PC card A7 (No. A65145-001), component location diagram.


Figure 5-9. PC card A14 (No. A65173-001), component location diagram.


Figure 5-10. PC card A15 (No. A65153-001), component location diagram.


Figure 5-11. PC card A5 (No. A65205-001), component location diagram.


Figure 5-12. PC card A1 (No. A65209-002), component location diagram.


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Figure 5-13. PC card A4 (No. A65215-001), component location diagram.


Figure 5-13.1. PC card A4 (A65223-001), component location diagram.


Figure 5-13.2. PC card A5 (A 65227-001), component location diagram.


Figure 5-14. PC card As (No. SME546659-001), component locution diagram.


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Figure 5-15. Power Supply PS1 component board assembly AI (+4.75 volt dc), component location diagram.


Figure 5-16. Power supply PS1 component board assembly A2 ( $\mathbf{\pm 1 2}$ volt dc), component location diagram.


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Figure 5-17. Power supply PS1 component board assembly AS (- 48 volt dc), component location diagram.


Figure 5-18. Power supply PS1 heat sink components assembly A4, component locations diagram.


Figure 5-19. Power supply PS1 heat sink components assembly A5.


Figure 5-20. Power supply PS1 heat sink components assembly A6.


Figure 5-21. Power supply PS1 sequence module component board assembly A12.
Change 3 5-22


Figure 5-22. Power Supply PS1 connector bracket assembly A14 and component board assembly A15.


Figure 5-23. Power Supply PS1 manual control card.

## CHAPTER 6

## DEPOT MAINTENANCE

## Section I. DEPOT REPAIR

## 6-1. General

Complete rebuild of the card reader may be accomplished by depot maintenance facilities, when authorized by appropriate authority. Rebuild action includes all repairs, rebuild, and replacement necessary to make this equipment equivalent to new material and suitable for return to the military supply system for reissue to using organizations.

## 6-2. Depot Repair

Depot repair includes all repair procedures described in chapters 4 and 5 , in addition to the part fabrication and refinishing procedures possible with the metalworking and refinishing equipment available at a depot.

## Section II. DEPOT OVERHAUL STANDARDS

## 6-3. Applicability of Depot Overhaul Standards

Reader, Punched Card RP-152/G (card reader) must be tested thoroughly after repair to insure that it meets adequate performance requirements for return to stock and reissue. Use the tests described in this section to measure the performance of the repaired device. Equipment that is to be returned to stock should meet all of the performance standards given in this section.

## 6-4. Applicable References

a. Repair Standards. Applicable procedures of the depots performing this test and the general standards for repaired equipment given in TB SIG 355-1, TB SIG $355-2$, and TB SIG $355-3$ form a part of the requirements for testing this equipment.
b. Technical Publications. The technical publications applicable to the equipment to be tested are listed in appendix A
c. Modification Work Orders. Perform the work specified by modification work orders pertaining to this equipment before making the tests specified. DA Pam 310-7 lists all available MWO's.

## 6-5. Test Facilities Required

In addition to the tools and test equipment listed in appendix C , the following special tools and test
equipment are required to perform the Depot Overhaul Standards Tests.

| Item | cription |
| :---: | :---: |
| Frequency Counter (2 required). | Beckman, Model 7350A, or equivalent; accuracy of 1 part in $10^{8}$ per week. |
| Card Reader Test Set. | General Dynamics Electronics Division Model 48-200711. |
| Timer, one minute. | Standard, TF-4570. |
| Regulated Power Amplifier. | CML Model N5000A, or equivalent, with $0.5 \%$ accuracy. |
| Plug-in Oscillator. | CML Model SG13A, or equivalent, with $0.25 \%$ accuracy. |
| Test Cable | Test cable terminated in 48-pin connector on one end and two fanning strips and a single No. 8 wire on other end. Cable is labeled "Reader" |
| Card Stack "A" | Consists of one hundred and eight (108) standard punch cards, white in color, punched in such a manner as to conform with the sequence of characters generated by the Card Reader Test Set. This sequence will be sixteen (16) asterisks followed by sixty-four (64) printable ASCII characters. See figure 6-1 and table 6-1. |
| Card Stack "B" | Consists of eleven hundred (1100) cards, one thousand (1000) white |

Item | Description |
| :--- |
| cards and one hundred (100) blue |
| cards. The cards will be punched in |
| the same manner as card stack "E" |
| and shall have the one thousand |
| (1000) white cards stacked together |
| followed by the one hundred (100) |
| blue cards. |
| (consists of one hundred and thirteen |
| (113) cards, one hundred and six |
| (106) cards, white in color and |
| seven (7) cards blue in color. The |
| cards in Card Stack "C" will be |
| arranged and punched in the |
| following order: |
| NOTE |

Card Stack "C"

Card Nos. 1 through 50: White in color, punched in the same manner as cards described in Stack "A". See figure 6-1.
Card No. 51: Blue in color, punched in the same. manner as cards in Stack "A", with the exception of Column 46. In this column Rows two (2) and seven (7) will be punched. This card will be marked "Invalid Character".
Card No. 52. White in color, punched in the same manner as cards described in Stack "A".
Card No. 53.: Blue in color, punched in the same manner as cards in Stack "A" with the exception of Column 47. In this column Rows five (5) and nine (9) will be punched. This card will be marked "Invalid Character".
Card No. 54: Same as Card No. 52.
Card No. 55: Blue in color, punched in the same manner as cards in Stack "A" with the exception of Column 48. In this column Rows ten (10), eleven (11), and nine (9) will be punched. This card will be marked "Invalid Character".
Card No. 56: Same as Card No. 52.
Card No. 57. Blue in color, punched in the same manner as cards in Stack "A" with the exception of Column 49. In this column Rows two (2), eight (8), and eleven (11) will be punched. This card will be marked "Invalid Character".
Card No. 58. Same as Card No. 52.
Card No. 59: Blue in color, punched in the same manner as cards in Stack "A" with the exception of Column 50. In this column Rows

## Description

eleven (11) and twelve (12) will be punched. This card will be marked "Invalid Character".
Card No. 60. Same as Card No. 52.
Card No. 61: Blue in color, punched in the same manner as cards in Stack "A" with the exception of Column 51. In this column Rows one (1) and eight (8) will be punched. This card will be marked "Invalid Character".
Card No. 62. Same as Card No. 52.
Card No. 63. Blue in color, punched in the same manner as cards in Stack "A" with a notch in the space preceding Column one (1), Row four (4). This notch will simulate a dark check failure. This card will be marked "Dark Check". Se figure 6-2.
Card Nos. 64 through 113: Same as Card No. 52.
Card Stack "D" Consists of 1000 white cards, punched in the following manner: one punch in Row 10 of Column 1, followed by punches in Rows 6 and 11 in Column 2. This sequence is repeated for the 80 columns.
Card Stack "E" $\begin{gathered}\text { Consists of } 200 \text { cards, } 108 \text { white cards } \\ \text { followed by } 92 \text { colored cards. The }\end{gathered}$ followed by 92 colored cards. The cards will be punched in such a manner as to conform with the sequence of characters generated by the Card Reader Test Set. This sequence will be 16 asterisk characters followed by 64 printable ASCII Code characters including each of the 62 punched card code assignments as shown in figure 6-3 and table 6-2
Card Stack "F"


Card Stack "H"
Consists of 118 cards, 108 white cards followed by 10 colored cards. The cards will be punched in such a manner as to conform with the sequence of characters generated by the Card Reader Test Set. This sequence will be 16 asterisk characters followed by 64 printable ASCII Code characters including each of the 62 punched card code assignments shown ih figure 6-3 and table 6-2
Card Stack "G"
Consists of two cards punched in the following manner: punches in Row 12 and Row 10 of each column as shown in figure 6-3.1.
Consists of two cards punched in the following manner: punches in Row 11 and Row 10 of each column as shown in figure 6-3.2.


#  




Figure 6-1. Test card, stack 'A'.


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Figure 6-2. Dark check test card.
 ITIC IIIIIII IHIHIIIHIII I II ! I IIIIII I II













TM7440-215-15-111

Figure 6-3. Test card, stack ' E '.

## 

## 

 22222222222222222222222222222222222222222222222222222222222222222222222222222212 3333333333333333333333333333333333333333333333333333333333333333333333333333



 8888888888888888888888888888888888888888888888888888888888 88888888888888888888888
 ——:

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Figure 6-3.1. Test card, stack 'G'.





``` 22222222222222222122222222222222222222222222221222222222122122222212221222212212 3 3 3 3 J 3 3 3 J 3 3 3 J J 3 J 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
```



``` 55555555555555555555555555555555555555555555555555555555555555555555555555595555
```




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Figure 6-3.2. Test card, stack 'H'
Table 6-1. Test Pattern Character Sequence

| Card column | Character | Punch code |
| :---: | :---: | :---: |
| 1 .......... | *Asterisk. | 11, 8, 4 |
| 2 .......... | *Asterisk. | 11, 8, 4 |
| 3 .......... | *Asterisk. | 11, 8, 4 |
| 4 | *Asterisk. | 11, 8, 4 |
| 5 | *Asterisk. | 11, 8, 4 |
| 6 | *Asterisk. | 11, 8, 4 |
| 7. | *Asterisk. | 11, 8, 4 |
|  | *Asterisk. | 11, 8, 4 |
|  | *Asterisk. | 11, 8, 4 |
| 10 | *Asterisk. | 11, 8, 4 |
| 11. | *Asterisk. | 11, 8, 4 |
| 12 | *Asterisk. | 11, 8, 4 |
| 13 | *Asterisk. | 11, 8, 4 |
| 14 | *Asterisk. | 11, 8, 4 |
| 15. | *Asterisk. | 11, 8, 4 |
| 16 | *Asterisk. | 11, 8, 4 |
| $17 . . . . . . . . .$. | Space. | No punches |
| 18 | ! exclamation point | 12, 8, 7 |
| $19 . . . . . . . .$. | "Quotation mark | 8, 7 |
|  | \# Number sign. | 8, 3 |
| 21. | \$ Dollar sign. | 11, 8, 3 |
| 22 | \%. Percent | 10, 8, 4 |
| 23 | \& Ampersand | 12 |
| 24 | ' Apostrophe.. | 8, 5 |
| 25 | ( Opening parenthesis | 12, 8, 5 |
| 26 | ) Closing parenthesis.. | 11, 8, 5 |
| 27. | *Asterisk. | 11, 8, 4 |
| 28 | + Plus. | 12, 8, 6 |
| $29 . . . . . . . .$. | , Comma | 10, 8, 3 |
| 30 .......... | - Hyphen | 11 |
| $31 . . . . . . . . .$. | . Period | 12, 8, 3 |
| $32 . . . . . . . .$. | / Slant | 10, 1 |
| 33 .......... | Ø Zero.. | 10 |
| 34 ........... | 1 | 1 |
| $35 . . . . . . . .$. | 2 | 2 |
| $36 . . . . . . . . .$. | 3. | 3 |
| 37 .......... | 4 .............................................................. | 4 |


| Table 6 Card column | 1. Test Pattern Characte | Punch code |
| :---: | :---: | :---: |
| 38 ........... | $5 . . . . . . . . . . .$. | 5 |
| 39 | 6 | 6 |
| 40 .......... | 7 | 7 |
| 41. | 8 | 8 |
| 42. | 9 | 9 |
| 43 ........... | : Colon | 8, 2 |
| 44 .......... | ; Semicolon. | 11, 8, 6 |
| $45 . . . . . . . .$. | < Less than | 12, 8, 4 |
| $46 . . . . . . . .$. | = Equal | 8, 6 |
| 47 .......... | > Greater than. | 10, 8,6 |
| 48 | ? Question mark. | 10,8,7 |
| 49 | @ Commercial at (') Note 1. | 8, 4 |
| 50 .......... | A. | 12, 1 |
| 51. | B. | 12, 2 |
| 52 | C. | 12, 3 |
| 53 ........... | D. | 12, 4 |
| $54 . .$. | E | - 12.5 |
| 55 | F | 12, 6 |
| 56 ........... | G. | 12, 7 |
| $57 . . . . . . . .$. | H. | 12. 8 |
| 58 | 1. | 12, 9 |
| 59 .......... | J.. | 11, 1 |
| 60 ........... | K. | 11, 2 |
| 61. | L. | 11, 3 |
| 62 .......... | M | 11, 4 |
| 63 .......... | N. | 11, 5 |
| 64 .......... | O. | 11, 6 |
| $65 . . . . . . . .$. | P | 11, 7 |
| 66 .......... | Q. | 11, 8 |
| $67 . . . . . . . .$. | R. | 11, 9 |
| 68. | S. | 10.'2 |
| 69. | T. | 10, 3 |
| $70 . . . . . . . .$. | U. | 10, 4 |
| $71 . . . . . . . .$. | V. | 10, 5 |
| 72. | W. | 10, 6 |
| 73. | X. | 10, 7 |
| 74 .......... | Y. | 10, 8 |
| $75 . . . . . . . .$. | Z | 10, 9 |
| $76 . . . . . . . .$. | ¢ Plus Zero ([) Note 1 | .11, 8, 4 |
| 77 ........... | $\backslash$ Reverse Slant ( ) Note 1 | .10, 8, 2 |
| $78 . . . . . . . .$. | Ō Minus Zero (]) Note $1 . .$. | .11, 8, 4 |
| $79 . . . . . . . .$. | ${ }^{\wedge}$ Circumflex ............. | 11, 8, 7 |
| 80 ........... | _ Underline........ | .10, 8,5 |

## Note 1: ( ) indicates AUTODIN printed character.

Table 6-2. Test Pattern Character Sequence


| Card column | Character | Punch code |
| :---: | :---: | :---: |
| 17 ........... | Space............................ | No punches |
| 18 .......... | ! exclamation point | 12, 8, 7 |
| $19 . . . . . . . .$. | "Quotation mark. | 8, 7 |
| $20 . . . . . . . .$. | \# Number sign. | 8, 3 |
| $21 . . . . . . . .$. | \$ Dollar sign. | 11, 8, 3 |
| 22. | \% Percent . | 10, 8, 4 |
| $23 . . . . . . . .$. | \& Ampersand | 12 |
| $24 . . . . . . . .$. | ' Apostrophe.. | 8, 5 |
| $25 . . . . . . . .$. | ( Opening parenthesis | 12, 8, 5 |
| 26 | ) Closing parenthesis. | 11, 8, 5 |
| 27 | *Asterisk... | 11, 8, 4 |
| $28 . . . . . . . .$. | + Plus.... | 12, 8, 6 |
| $29 . . . . . . . .$. | , Comma | 10, 8, 3 |
| $30 . . . . . . . .$. | - Hyphen | 11 |
| $31 . . . . . . . .$. | . Period ... | 12, 8, 3 |
| 32 | / Slant | 10, 1 |
| $33 . . . . . . . .$. | Ø Zero.. | 10 |
| 34 .......... | 1 ... | 1 |
| $35 . . . . . . . .$. | 2 | 2 |
| $36 . . . . . . . .$. | 3 | 3 |
| 37 ........... | 4 | 4 |
| $38 . . . . . . . .$. | 5 | 5 |
| 39 .......... | 6 | 6 |
| 40 .......... | 7 | 7 |
| 41 ........... | 8 | 8 |
| 42 ........... | 9 | 9 |
| 43 ........... | : Colon | 8, 2 |
| $44 . . . . . . . .$. | ; Semicolon. | 11, 8, 6 |
| $45 . . . . . . . . .$. | < Less than | 12, 8, 4 |
| 46 .......... | = Equal | 8, 6 |
| $47 . . . . . . . .$. | > Greater than.. | 10, 8,6 |
| 48 ........... | ? Question mark. | 10, 8,7 |
| $49 . . . . . . . .$. | @ Commercial at (`) Note 1. | 8, 4 |
| $50 . . . . . . . . .$. | A ............................ | 12, 1 |
| $51 . . . . . . . . .$. | B. | 12, 2 |
| $52 . . . . . . . .$. | C. | 12, 3 |
| 53 ........... | D. | 12, 4 |
| 54 ........... | E. | - 12.5 |
| $55 . . . . . . . . .$. | F | 12, 6 |
| $56 . . . . . . . . .$. | G. | 12, 7 |
| 57 ........... | H. | 12. 8 |
| $58 . . . . . . . . .$. | 1. | 12, 9 |
| $59 . . . . . . . . . .$. | J. | 11, 1 |
| 60 ........... | K. | 11, 2 |
| 61 ........... | L. | 11, 3 |
| 62 ............ | M | 11, 4 |
| 63 ........... | N. | 11, 5 |
| 64 ........... | O.. | 11, 6 |
| $65 . . . . . . . . .$. | P. | 11, 7 |
| 66 ........... | Q. | 11, 8 |
| $67 . . . . . . . . .$. | R. | 11, 9 |
| 68 ........... | S. | 10, 2 |
| $69 . . . . . . . . .$. | T. | 10, 3 |
| 70 ........... | U. | 10, 4 |
| 71 ........... | V. | 10, 5 |
| $72 . . . . . . . . .$. | W | 10, 6 |
| 73 ........... | X | 10, 7 |
| $74 . . . . . . . .$. | Y. | 10, 8 |
| $75 . . . . . . . . .$. | Z | 10, 9 |
| $76 . . . . . . . . .$. | *Asterisk.. | 11, 8, 4 |
| $77 . . . . . . . . .$. | \ Reverse Slant ( ) Note 1 | 10, 8, 2 |
| $78 . . . . . . . . .$. |  | 11, 8, 4 |
| $79 . . . . . . . . .$. | $\wedge$ Circumflex | 11, 8, 7 |
| 80 .......... | _ Underline....................... | 10, 8, 5 |

## 6-6. General Test Conditions and Requirements

Before the tests (para 6-7 through 6-9) are made, the equipment shall meet the mechanical requirements specified in a below. The general test conditions of below shall be established.
a. Mechanical Requirements.
(1) The card reader should be assembled for 120 VAC, 60 Hertz operation, and should be adjusted to meet the requirements of paragraphs 4-50 through 4-70.
(2) Muffler and jar element should be cleaned per the procedures of paragraph 4-9 before starting the tests of this section.

## b. Test Conditions.

(1) Unless otherwise specified, all tests will be performed under the following test conditions:

| Temperature. | Ambient $15^{\circ} \mathrm{C}$. To $35^{\circ} \mathrm{C}$ |
| :--- | :--- |
| Altitude | Normal ground |
| Humidity | Room ambient up to $98 \%$ |
| Power | 120 VAC. 60 hertz |

(2) Connect the card reader to the test equipment as shown in figure 6-4
c. Test Set Modification. To permit use of the Test Set, General Dynamics Model 48-200711 to check the card reader after incorporation of Federal Standard FIPS-14 Card Code, MWO 11-7440-215-30-2, modification to the test set is required. Modified card readers generate ASCII codes of 11111011 and 11111101 for the opening bracket ([) and closing bracket (]) characters to represent the plus-zero ( $\partial$ ) and minuszero ( $\overline{0}$ ) characters respectively. These ASCII codes are out of the binary sequence of the internal counter in the test set and action must be taken to mask these characters or a comparison error will result. Proceed as follows to modify the test set:
(1) Refer to figure 6-3.3 and make the following wiring changes on test set printed circuit card A11:
(a) At Z7D remove the connections to Z7D-3 and Z7D-4 from Z5A-2.
(b) At Z7D make connections from Z7D-3 and Z7D-4 to Z7D-5.
(c) At $Z 5 \mathrm{~A}$ remove the connections to Z5A-7 from Z4D-10 and to Z5A-9 from Z4B-2.
(d) Check, and if necessary, make a connection from Z4B-2 to A11-pin AA as shown on figure 6-3.3.
(e) At Z5A make connections from Z5A-7 to Z3C-2 and from Z5A-8 to Z5A-9.
(f) At Z3C remove the connections from Z3C-5 to A11-pin 12, from Z3C-9 to A11-pin 8, and from Z3C-10 to A11-pin 9. If any of the above terminals on Z3C have more than one wire connected to the terminal, reconnect the wires after removal from Z3C to assure continuity of the signal. Use spare pads on the PC card provided for this purpose.
(g) At Z3C make connections from Z3C-5 to A11-pin 5, from Z3C-9 to A11-pin 15, and from Z3C-10 to A11-pin 16.
(2) Use an ohmmeter or continuity tester and verify the connections to $\mathrm{Z3C}, \mathrm{Z4A}, \mathrm{Z4B}, \mathrm{Z5A}$, and $\mathrm{Z7D}$ as shown. Other decode circuitry originally inputting signals to Z7D are now disabled. This circuitry was originally used to decode for 14 different characters which were invalid in early AUTODIN equipment which conflicted with the FIELD DATA code used in the AUTODIN switches. (3) On the test set logic assembly, disable the CR TEST CARDS/HSCP CARDS switch as follows (fig. 6-3.3):
(a) Remove the connection from XA11-
$F$ to the switch.
(b) Remove the connection from XA177 to the switch.
(c) Make a connection between XA11-F
to XA17-7.

## Change 6 6-6.2



Figure 6-3.3. Test Set Model 48-200711 modification.
Change 6-6.3

## 6-7. Visual Tests

Disconnect power from the device. Check the general physical condition of the equipment as follows:
a. Exterior and Interior Surfaces. All surface finishes must be free from rust, scratches or other damage. Surfaces must not be damaged.
b. Cables. The lead connections of all cables must
be secure. All cable connectors must be undamaged and cables should not be cracked, frayed, or routed to place strain on the wires.
c. Hardware. All bolts and screws, such as slide mounting screws, panel mounting screws, motor mounting bolts and mechanism mounting screws must be tight.


Figure 6-4. Test setup.

## Change 6 6-6.4

d. PC Cards. Check that all printed circuit cards in logic assembly A1 are mounted securely in the proper connector (para 1-6).

## 6-8. Operational Tests - Fixed Voltage and Frequency

## a. Preliminary Procedure.

(1) Set the switches and controls on the Card Reader Test Set (test set) as follows:

115 VAC circuit breaker to OFF
CANCEL to OFF
SYNC FAIL to OFF
EOM to OFF
SELECT to off
SINGLE CARD/REPEAT to REPEAT
COMPARATOR INPUT rotary switch to DATA I
AUTO/MAN to AUTO
COMPARATOR IN/OUT to OUT ASSIGNED/NOT ASSIGNED to NOT ASSIGNED
(2) Position the POWER switch on the variable frequency and voltage source (CML N5000A) to ON and allow a five-minute warm-up.
(3) Position the HIGH VOLTAGE switch on the variable frequency and voltage source to ON.
(4) Adjust the OUTPUT LEVEL control on the variable frequency and voltage source to produce a reading of 120 VAC on the OUTPUT VOLTAGE meter. Adjust the frequency control for 60 CPS .
(5) Position the 115 VAC circuit breaker switch on the test set to ON and verify that the test set AC on lamp lights.
(6) With current limiting controls set fully clockwise, check that test set dc power supplies are supplying proper voltage output levels:

$$
\begin{aligned}
& +4.75 \mathrm{VDC} \pm 0.1 \mathrm{VDC} \\
& \text { + 12.0 VDC } \pm 0.1 \mathrm{VDC} \\
& \text { - } 12.0 \mathrm{VDC} \pm 0.1 \mathrm{VDC}
\end{aligned}
$$

(7) Press the AC POWER switch on the card reader (CR) and verify that the switches and indicators light as follows:

AC POWER switch $\qquad$ white
DC POWER indicator $\qquad$ white
STOP switch
h.

NOT ASSIGNED indicator red

CARD ALARM indicator. $\qquad$ amber
(8) Verify that the reader mechanism motor is operating.
(9) Verify that the blower in the CR cabinet is operating.
(10) Press the card reader AC POWER switch and verify the following results:
(a) No CR switches or indicators are illuminated.
(b) Reader mechanism drive motor is not operating.
(c) Blower in CR cabinet is not operating.
(11) Remove the two 15 VAC LAMP fuses from the CR power supply.
(12) Press the AC POWER switch on the CR and verify the following results:
(a) Card reader DC POWER indicator illuminates, but all other indicators and switches are out.
(b) Reader mechanism drive motor is operating.
(c) Blower in CR cabinet is operating.
(13) Press the card reader AC POWER switch and replace the 15 VAC LAMP fuses.
(14) Remove the 120 VAC 10 A DRIVE MOT fuse from the CR power supply.
(15) Press the AC POWER switch on the CR and verify the following:
(a) AC POWER switch, DC POWER indicator and STOP switch, indicators are lit.
(b) Blower in CR cabinet is operating.
(c) Reader mechanism drive motor is not operating.
(16) Press the AC POWER switch on the CR and replace the DRIVE MOT fuse.
(17) Remove the 120 VAC 3 A FAN fuse from the CR power supply.
(18) Press the AC POWER switch and verify the following:
(a) AC POWER switch, DC POWER indicator and STOP switch, indicators are lit.
(b) Reader mechanism drive motor is operating.
(c) Blower in CR cabinet is not operating.
(19) Press the AC POWER switch on the CR and replace the FAN fuse.
(20) Remove the 120 VAC PWR SUP INPUT fuse from the CR power supply.
(21) Press the AC POWER switch on the CR and verify the following:
(a) No switches or indicators on the CR are illuminated.
(b) Reader mechanism drive motor is not operating.
(c) Blower in CR cabinet is not operating.
(22) Replace the PWR SUP INPUT fuse and remove the +4.75 VDC fuse.

## NOTE

Following depression of the AC POWER switch (step 23), the drive mechanism motor may run and the blower may operate, and switches and indicators may light momentarily until the power supply shuts off. The conditions of step (23) (a) through (c) should be observed within seven seconds after the AC POWER switch is operated.
(23) Press the AC POWER switch on the CR and observe the following:
(a) No switches or indicators on the CR are illuminated.
(b) Reader mechanism drive motor is not operating.
(c) Blower in CR cabinet is not operating.
(24) Replace the +4.75 VDC fuse in the power supply.
(25) Remove the +12 VDC, -12 VDC and -48 VDC fuses from the power supply, one at a time, repeating step 23 each time.
(26) With all fuses installed in the power supply, press the AC POWER switch on the CR. Verify that the AC POWER switch, DC POWER indicator, and STOP switch, indicators are lit. Drive mechanism motor should be running and blower in CR cabinet should be operating.
b. Lamp Test. Press the LAMP TEST switch on the control panel of the PTR and verify that the following indicators light:

| Switch/Indicator | Color <br> NOT ASSIGNED ..................... <br> amber |
| :--- | :--- |
| PICK FAIL............................................... |  |
| red |  |

## NOTE

The AC POWER and DC POWER Indicators will remain white during the test. They are not tested by the LAMP TEST pushbutton switch.
c. Not Assigned Operation.
(1) Single feed.
(a) Load card stack ' $A$ ' in the card reader. Verify that CARD ALARM indicator is extinguished, and all other indicators do not change condition.
(b) Press SINGLE FEED switch on the card reader. Verify that STOP switch is extinguished and SINGLE FEED switch lights momentarily as one card feeds from hopper to stacker.
(c) Verify that SINGLE FEED switch is extinguished and STOP switch illuminates after the card cycle is completed.
(d) Repeat this cycle (steps (b) and (c) ) for ten cycles, and verify that the mechanical components involved in card feeding operate smoothly without any binding or jamming. Also verify that the test set COMPARATOR INPUTS lamps do not change state during the single feed cycle.
(2) Card reader speed.
(a) Remove all cards from the card reader stacker and load in the hopper. Verify that all indications remain the same.

NOTE
Before performing step 6-8c(2) (b), read steps $6-8 c(2)$ (c) and (d).
(b) Press the card reader LOCAL TEST switch and start the one-minute timer. Verify that STOP switch is extinguished, LOCAL TEST switch lights, other switches and indicators do not change condition, and cards are fed automatically and continuously from hopper to stacker.
(c) While cards are being read (step 6$8 c(2)(b))$, press each of the following switches: START, SINGLE FEED, LAMP TEST. Verify that pressing these switches has no effect on the processing of cards, and other switches or indicators light only when the LAMP TEST switch is pressed. Also verify that the test set COMPARATOR INPUTS lamps do not change state.
(d) After the last card has been read, verify that the LOCAL TEST switch extinguishes, the STOP switch lights, and the CARD ALARM indicator lights. Stop the one-minute timer and verify that the card stack was read in one minute maximum.
(e) Remove card stack 'A' from the stacker. Examine the edges of the cards in the stack for damage which would prevent rereading the cards. Examine at least five cards at random for torn webbing
between punched holes. There should be no damage or torn webbing on the cards.
(3) START switch interaction.
(a) Remove card stack ' A ' from the stacker. Load hopper with the 1000 white cards of stack ' D '. Verify that CARD ALARM indicator on card reader is extinguished and other indicators and switches do not change condition.
(b) Press START switch on card reader. Verify that STOP switch is extinguished, START switch lights green, and test set RDY lamp lights green. Verify that no cards are read.
(c) With card reader in 'START green' condition, press each of the following switches: LOCAL TEST, SINGLE FEED, and LAMP TEST. Verify that operation of these switches has no effect on the card reader, and other indicators and switches are illuminated or extinguished only when the LAMP TEST switch is pressed.
(d) Press STOP switch on the card reader. Verify that the START switch is extinguished, the STOP switch lights, and other switches and indicators do not change condition. Verify that the test set RDY lamp goes out.
d. Assigned Operation.
(1) Data line and strobe waveforms.
(a) Connect test set DATA LINE TEST POINT 1 to channel A input of oscilloscope. Trigger the
oscilloscope internally on the pulse to be observed and adjust the oscilloscope controls to observe a waveform as shown in figure 6-5.
(b) Press the START switch on the CR. Press the START switch on the test set and observe the pulse displayed on the oscilloscope. Pulse displayed should have the following parameters:

| High level: | $+6.0 \pm 1.0 \mathrm{VDC}$ |
| :--- | ---: |
| Low level: | $-6.0 \pm 1.0 \mathrm{VDC}$ |
| Rise time: | 21 to $35 \mu \mathrm{sec}$ |
| Fall time: | 21 to $35 \mu \mathrm{sec}$ |

(c) Connect the channel A input of the oscilloscope to the test set DATA LINE TEST POINTS 2 through 7, and the $P$ (parity) test points in numerical sequence. Verify that the pulses displayed meet the parameters listed in step d (1) (b) above.
(d) Connect the channel A input of the oscilloscope to the test set STROBE test point. Verify that the strobe pulse also meets the parameters listed in step $d(1)(b)$ above.
(e) Press the CR STOP switch. Remove all cards from stacker and reload in hopper.
(f) Connect the channel A input of the oscilloscope to the test set DATA LINE TEST POINT 1, and connect the channel B input of the oscilloscope to


Figure 6-5. Data pulse and data strobe waveform.
Change 4 6-9
the STROBE test point. Set the oscilloscope to the STROBE test point. Set the oscilloscope controls for chopped operation, using the data pulse as an external trigger. Press the CR START switch and the test set START switch. Verify that the position of the strobe pulse relative to the data pulse conforms to the limits shown in figure 6-6.
(g) Press the card reader STOP switch.
(h) Disconnect the oscilloscope from the STROBE test point and DATA LINE TEST POINTS on the test set. Connect channel A of the oscilloscope to the STEP test point.
(i) Press the START switch on the CR.
(j) Press the test set START switch.
(k) Verify that the signal levels observed on the oscilloscope are polar, with a nominal +6 VDC high level and a nominal -6 VDC high level.
(I) Press the card reader STOP switch and disconnect the oscilloscope. Remove all cards from the hopper and stacker.
(2) Data verification.
(a) Remove card stack 'D' from stacker and hopper and load card stack 'B'.
(b) Place ASSIGNED/NOT ASSIGNED switch on the test set to the ASSIGNED position. Verify that NOT ASSIGNED indicator on the card reader is extinguished and other indicators and switches on the card readers do not change position.
(c) Connect oscilloscope channel A input to test set ASSIGN test point. Position oscilloscope controls to observe a dc level and verify a reading of $0.5 \pm 0.5 \mathrm{VDC}$ with the ASSIGNED/NOT ASSIGNED switch in the ASSIGNED position.
(d) Place the test set ASSIGNED/NOT ASSIGNED switch to the NOT ASSIGNED position. Verify a voltage level of $6.0 \mathrm{VDC} \pm 1.0 \mathrm{VDC}$.
(e) Place ASSIGNED/NOT ASSIGNED switch to the ASSIGNED position. Verify that voltage level returns to the level of step (c) above.

## NOTE

The following steps verify accurate data transfer between the card reader and test set. This is done automatically in the test set when the COMPARATOR IN/OUT switch is in the IN position. Comparison is made of the information generated in the test set with information coming from the punched cards being read by the card reader. This comparison is indicated by the changing status of the eight COMPARATOR INPUTS lamps when the COMPARATOR INPUTS switch is placed in the DATA- IN position. These lamps are designated 1 through 7, with the


Figure 6-6. Data strobe versus data pulse timing.
eighth lamp designated ' $P$ ' (parity). If incorrect data is received from the card reader, the ERR (error) lamp on the test set will light red and the card reader will go to a stop condition.
(f) Press the START switch on the card reader. Verify that the STOP switch on CR is extinguished, START switch lights green, test set RDY lamp lights green, and all other switches and indicators do not change condition.
(g) Place SELECT switch on test set to ON.
(h) Connect oscilloscope channel A input to SELECT test point on the test set. Verify a voltage level of $+0.5 \pm 0.5 \mathrm{VDC}$.
(i) Place the SELECT switch to the off position. Verify a voltage level of $+6.0 \pm 1.0 \mathrm{VDC}$ at the SELECT test point.
(J) Return the test set SELECT switch to the ON position.
(k) Connect oscilloscope channel A input to test set RDY test point. Verify a voltage level of $0.5 \pm 0.5 \mathrm{VDC}$.
() Press the card reader STOP switch and verify a voltage level of $6.0 \pm 1.0 \mathrm{VDC}$ at the RDY test point.
( $m$ ) Press the card reader START switch and place the COMPARATOR IN/OUT switch on the test set to IN .

> NOTE
> When the COMPARATOR IN/OUT switch is set to IN, the ERR lamp on the test set will light, because synchronization between the generated test pattern and the input data is not established until step ( $n$ ) below.
(n) Press START switch on test set. Verify that START switch on card reader changes from green to white and that cards feed automatically and continuously from hopper to stacker. Verify that the ERR lamp on the test set is extinguished and that all COMPARATOR INPUTS lamps are changing state with COMPARATOR INPUTS switch in the DATA IN position.
(o) While cards are being read, press the following switches: LOCAL TEST, SINGLE FEED, and LAMP TEST. Verify that the use of these switches does not affect operation on the card reader, and that additional switches and indicators are illuminated or extinguished only when the LAMP TEST switch is pressed.
(p) Press STOP switch on card reader. Verify that the card reader stops and that START switch
indicator is extinguished, STOP switch lights, and other switches and indicators on card reader do not change condition. Verify that RDY lamp on test set is out.
(q) Verify that bottom card (and only bottom card) in the CR stacker is offset one quarter inch minimum from the card above it.
(r) Remove card stack "B" from the stacker and the hopper and load card stack "G" in the hopper.
(s) On the test set burn the COMPARATOR INPUT rotary switch to DATA COMP. On the card reader press the START switch and the ALARM RESET switch.
( $t$ ) Press the START switch on the test set. Verify the card reader reads one card and the STOP switch lights red. On the test set verify the ALM and ERR lamps are lit and the COMPARATOR INPUTS lamp indicate 11111011.
(u) Remove card stack "G" from the stacker and the hopper and load card stack " H " in the hopper.
(v) On the card reader press the START switch and the ALARM RESET switch.
(w) Press the START switch on the test set. Verify the card reader reads one card and the STOP switch lights red. On the test set verify the ALM and ERR lamps are lit and the COMPARATOR INPUTS lamps indicate 11111101.
(x) On the test set place the COMPARATOR INPUT rotary switch to DATA IN and set the COMPARATOR IN/OUT switch to OUT.
(y) Remove card stack "H" from the stacker and the hopper and load card stack " B " in the hopper.
(3) Single feed.
(a) Press the card reader SINGLE FEED switch. Verify that the CR STOP switch is extinguished, SINGLE FEED switch lights, and all other switches and indicators do not change condition. Also verify that RDY and ERR lamps on test set light.

NOTE
The ERR lamp on the test set lights because synchronization between the test set and CR is lost. Synchronization is reestablished at step (c) below.
(b) With the card reader in single feed condition, press the following switches: START, LOCAL TEST, LAMP TEST. Verify that the operation of these switches has no effect on the card reader, and that additional switches and indicators are illuminated or extinguished only when the LAMP TEST switch is pressed.
(c) With the card reader still in the
single feed condition press the START switch on the test set. Verify that only one card is fed from hopper to stacker, SINGLE FEED switch is extinguished, STOP switch lights, and other switches and indicators on CR do not change condition. Also verify that RDY lamp on test set is extinguished. During the single feed cycle, verify that the test set COMPARATOR INPUTS lamps change state.
(4) EOM and EOB.
(a) Connect oscilloscope channel A input to the EOM test point on the test set.
(b) Place the EOM switch on the test set to ON.
(c) Position the oscilloscope controls to view a 60 millisecond pulse with a negatively sloped leading edge. Trigger the oscilloscope internally on the signal being viewed.
(d) Press the START switch on the card reader. Verify that STOP switch is extinguished, START switch lights white, and all other switches and indicators on CR do not change condition. Also verify that RDY lamp on test set lights.
(e) Press the START switch on the test set and verify that cards feed from hopper to stacker on card reader.
(f) Verify that the pulse at the EOM test point has a high level of $+6.0 \pm 1.0$ VDC (starting and finishing level), and a low level of $0.5 \pm 0.5 \mathrm{VDC}$ during the pulse time.
(g) Connect oscilloscope channel A input to the EOB test point on the test set.
(h) Verify that the pulse at the EOB test point has a high level of $+6.0 \pm 1.0$ VDC (starting and finishing level) and a low level of $0.5 \pm 0.5 \mathrm{VDC}$ during the pulse time.
(i) Allow cards to run until hopper is empty. Verify that all cards are read without producing an error indication on the test set.
(j) Verify that the START switch and CARD ALARM indicators are not illuminated, and the STOP switch it illuminated on the card reader. Verify that all other switches and indicators on the CR do not change condition.
(k) On the test set, verify that the OP ALM, ALM STOP and RDY lamps are extinguished.
e. Alarm Conditions.
(1) Stacker full.
(a) Place the remaining 100 blue cards from card stack 'B' into the hopper. Verify that no switches or indicators on the card reader or test set change condition.
(b) Connect oscilloscope channel A input to the OP ALM test point on the test set. Verify a voltage level of $0.5 \pm 0.5 \mathrm{VDC}$.
(c) Press START switch on CR. Verify that STOP switch extinguishes, START switch lights white, and all other switches and indicators do not change condition. Also verify that test set RDY lamp lights green.
(d) Press START switch on test set. Allow cards to process to a stacker full condition. Verify that the stacker full condition causes the card reader to stop processing cards and causes the CARD ALARM indicator to light, the START switch to go out, and the STOP switch to light. Other switches and indicators on the CR should remain unchanged. Also verify that the RDY and ERR lamps on the test set are not lit, but the OP ALM is illuminated.
(e) Verify that the oscilloscope indicates a voltage level of $+6.0 \pm 1.0 \mathrm{VDC}$ at the OP ALM test point.
(f) Press the START switch on the CR. Verify that no change in CR switches or indicators occurs, and no cards are read.
(g) Remove all cards from the stacker. Verify that no change in card reader switches or indicators occurs.
(h) Press START switch on card reader. Verify that the CARD ALARM indicator extinguishes, the START switch lights white, and the test set RDY lamp lights.
(i) Connect oscilloscope channel A input to the ALM RST test point on the test set. Adjust oscilloscope controls to view a $5 \mu \mathrm{sec}$ wide negative going pulse. Use the pulse being viewed as an external trigger.
(j) Press the AUDIBLE RESET switch on the card reader. Verify that the OP ALM lamp on the test set goes out. Press the AUDIBLE RESET switch as necessary to verify that the audible reset pulse is $5 \mu \mathrm{sec}$ minimum in duration, with an amplitude of $6.0 \pm 1.0 \mathrm{VDC}$ at its high level (starting and ending level), and $0.5 \pm 0.5$ VDC at its low level during the pulse time.
(k) Remove the remaining cards from the card reader hopper. Verify that the START switch and the test set RDY lamp extinguish, and the card reader STOP switch lights.
(2) Pick fail.
(a) Place the special pick-fail card (fig. 6-7) in the card reader hopper, with several cards placed on top of it.
(b) Press START switch on card reader. Verify that STOP switch is extinguished and START switch lights white. Also verify that RDY lamp lights and alarm lamps on test set are out.
(c) Press START switch on the test set. Verify that START switch is extinguished and STOP switch and PICK FAIL indicator are illuminated on the card reader. Verify that RDY lamp is extinguished and OP ALM lamp is illuminated on the test set. Verify that no cards are picked.
(d) Press the card reader START switch. Verify that the PICK FAIL indicator is extinguished, the START switch is illuminated white, and the test set RDY lamp is illuminated.
(e) Press the AUDIBLE RESET switch on the card reader. Verify that the OP ALM lamp is extinguished on the test set.
( $f$ ) Remove all cards from the hopper.


Figure 6-7. Pick-fail card.

Verify that the CARD ALARM indicator is illuminated, the STOP switch is illuminated, and the START switch is extinguished on the card reader. Verify that the lamp is extinguished and the OP ALM lamp is illuminated on the test set.
(3) Cancel.
(a) Load card stack ' C ' in the hopper.

Verify that no change occurs in test set or card reader indications.
(b) Connect oscilloscope channel A input to the CNCL test point on the test set. Verify a voltage reading of $0.5 \pm 0.5 \mathrm{VDC}$.
(c) Press START switch on card reader. Verify that STOP switch and CARD ALARM indicators on CR go out and START switch lights white. Verify that RDY lamp on test set lights.
(d) Press the AUDIBLE RESET switch on the card reader. Verify that OP ALM lamp on test set extinguishes.

## NOTE

The CANCEL switch must be actuated (step (f)) within 15 seconds after the test set start switch is pressed (step (e) ).
(e) Press START switch on test set and verify that cards feed from hopper to stacker.
(f) While cards are being read, place CANCEL switch on test set to MAN. Verify that cards stop feeding, the START switch on the CR goes out and the STOP switch and CANCEL indicators light. On the
test set verify that the RDY lamp goes out and the ALM STOP lamp lights.
(g) Verify that oscilloscope indicates a voltage level of $6.0 \pm 1.0 \mathrm{VDC}$ at CNCL test point.
(h) Press START switch on card reader. Verify that this switch has no effect with cancel applied.
(i) Place the test set CANCEL switch to the AUTO position.
() Press the card reader START switch. Verify that the STOP switch and CANCEL indicator are extinguished and the START switch is illuminated white. Verify that the RDY lamp is illuminated on the test set.
(k) Depress the AUDIBLE RESET switch on the card reader. Verify that the ALM STOP lamp is extinguished on the test set.

## NOTE

> The following steps demonstrate the use of the maintenance RESET switch.
(I) Place the CANCEL switch on the test set to the MAN position. Verify that START switch is extinguished and the STOP switch and CANCEL indicator are illuminated on the card reader. Verify that the ALM STOP lamp is illuminated and the RDY lamp is extinguished on the test set.
( $m$ ) Open the card reader front door to
gain access to the maintenance panel. Press the RESET switch on the maintenance panel. Verify that this action has no effect.
(n) Place the ASSIGNED/NOT ASSIGNED switch on the test set to the NOT ASSIGNED position. Verify that the NOT ASSIGNED indicator on the card reader is illuminated.
(o) Press the RESET switch on the maintenance panel of the card reader. Verify that the CANCEL indicator is extinguished.
(p) Place the test set CANCEL switch to the AUTO position.
(q) Place the ASSIGNED/NOT ASSIGNED switch on the test set to the ASSIGNED position. Verify that the NOT ASSIGNED indicator on the card reader is extinguished.
( $r$ ) Depress the START switch on the card reader. Verify that the STOP switch is extinguished and the START switch is illuminated green on the card reader. Verify that the RDY lamp is illuminated on the test set.
(s) Depress the AUDIBLE RESET switch on the card reader. Verify that the ALM STOP lamp is extinguished on the test set.
( $t$ ) Close the door to the maintenance panel on the card reader.

## (4) Invalid character.

(a) Connect oscilloscope channel A input to ALM STOP test point on test set. Verify that voltage level is $0.5 \pm 0.5 \mathrm{VDC}$.
(b) Press START switch on test set and verify the following:

1. Card reader START switch changes from green to white and cards process from hopper to stacker.
2. First card read is offset minimum of one-quarter inch from cards above it in stacker.
3. Cards are processed until card no. 51, containing an invalid character is read.
4. When the invalid character card is read, the CR stops processing cards with the START switch extinguished and the STOP and INVALID CHARACTER indicators illuminated.
5. When card reader stops, RDY and ALM STOP lamps on test set light.
6. When card reader stops, oscilloscope indicates voltage level of $6.0 \pm 1.0 \mathrm{VDC}$.
(c) Press card reader START switch. Verify that STOP switch and INVALID CHARACTER
indicators go out, and START switch lights white. Verify that RDY lamp on test set lights.
(d) Press AUDIBLE RESET switch on card reader and verify that all alarm lamps on test set go out.
(e) Repeat the above steps until all six invalid character cards in card stack 'C' have been read and detected.
(5) Photocell check.
(a) Following step 6-8e(4)(e) performed for the sixth invalid character card (No. 61), depress START switch on the test set. Verify that cards feed until the card reader PHOTOCELL CHECK indicator is illuminated and the card reader goes to a stop condition. Verify that the "Dark Check" card is the top card in stacker, and thus, the last card to be read. Verify that START switch is extinguished and STOP switch and PHOTOCELL CHECK indicator are illuminated on the card reader. Also verify ALM STOP lamp is illuminated and RDY lamp is extinguished on the test set.
(b) Remove the mechanism cover from the card reader.
(c) Depress START switch and AUDIBLE RESET switch on the card reader. Verify that STOP switch and PHOTOCELL CHECK indicator are extinguished, and START switch is illuminated white. Verify all alarm lamps extinguished and RDY lamp illuminated on the test set.
(d) Insert a strip of opaque paper between the lamp block and photocells in the read head. Cover any number of the twelve (12) read cells. Do not cover the BOC or EOC photocells. Verify that START switch is extinguished, STOP switch and PHOTOCELL CHECK indicator are illuminated on the card reader. Verify that RDY lamp is extinguished and ALM STOP lamp illuminated on the test set.
(e) Remove opaque paper. Verify no change in card reader or test set conditions from step 6$8 e(5)$ (d) above.
(6) Card jam.
(a) Depress START switch and AUDIBLE RESET switch on the card reader. Verify that STOP switch and PHOTOCELL CHECK indicator are extinguished and START switch is illuminated white. Verify all alarm lamps are extinguished and RDY lamp is illuminated on the test set.
(b) Hold the eraser end of a lead pencil two inches (2") upstream from the card reader offset capstan in a position to stop a card. While holding the pencil in this position, depress the START switch on

## Change 4 6-14

the test set. Verify that one card is picked and stops at the pencil, START switch is extinguished, and STOP switch and CARD JAM indicator are illuminated on the card reader. Verify that RDY lamp is extinguished and ALM STOP lamp is illuminated on the test set.

## NOTE <br> Card reader INVALID CHARACTER indicator may also illuminate as a result of the card jam.

(c) Allow the card that was jammed to pass into the stacker. Remove if from the stacker and discard.
(d) Depress the START switch on the card reader. Verify that the STOP switch and CARD JAM indicator are extinguished and the START switch is illuminated white on the card reader. Verify that the RDY lamp is illuminated on the test set.
(e) Depress the AUDIBLE RESET switch on the card reader. Verify that the ALM STOP lamp on the test set is extinguished.
(7) Out of sync.

## NOTE

The SYNC FAIL switch must be activated within 15 seconds after the test set START switch is depressed.
(a) Depress the START switch on the test set. Verify that cards are picked and fed automatically and continuously from hopper to stacker.
(b) While cards are being read, place SYNC FAIL switch on test set to the on position. Verify that cards stop feeding and that START switch is extinguished, and STOP switch and OUT OF SYN indicator are illuminated on the card reader. Also verify that RDY lamp is extinguished and ALM STOP lamp is illuminated on the test set.
(c) Depress START switch on the card reader. Verify that STOP switch and OUT OF SYN indicator are extinguished, START switch is illuminated white and all other indicators and switches do not change condition. Verify that RDY lamp is illuminated on test set and that no cards are processed.
(d) Depress AUDIBLE RESET switch on the card reader. Verify that all alarm lamps are extinguished on the test set.
(e) Place SYNC FAIL switch on test set to the OFF position.
(f) Hold remaining cards in hopper so that a card cannot be picked, but do not remove cards from hopper. Depress START switch on the test set. Verify that no card is picked, STOP switch and PICK FAIL indicator are illuminated and START switch is extinguished on the card reader. Verify that test set RDY lamp is extinguished and OP ALM lamp is illuminated.
(g) Using the hand, tap bottom of picker solenoid in order to manually pick one card. Verify that OUT OF SYN indicator illuminates and all other indicators and switches on card reader do not change condition. Also verify that ALM STOP lamp illuminates on the test set.
(8) Card alarm - hopper empty without EOM.
(a) Place EOM switch on the test set to the OFF position.
(b) Depress the START switch and AUDIBLE RESET switch on the card reader. Verify that STOP switch, OUT OF SYNC indicator and PICK FAIL indicator are extinguished. Verify that START switch is illuminated white. Verify that RDY lamp is illuminated and all alarm lamps are extinguished on the test set.
(c) Depress START switch on the test set and allow cards to feed until hopper is empty. Verify that the STOP switch and CARD ALARM indicator are illuminated and the START switch is extinguished on the card reader. Also verify that the test set RDY lamp is extinguished and OP ALM lamp is illuminated.
(d) Remove cards from stacker and reload in hopper. Verify no change in condition of card reader indications.
(e) Depress SINGLE FEED switch on the card reader. Verify that STOP switch and CARD ALARM indicator are extinguished and SINGLE FEED switch is illuminated white. Verify that the test set RDY lamp is illuminated.
( $f$ ) Depress the AUDIBLE RESET switch on the card reader. Verify that the OP ALM lamp is extinguished on the test set.
(g) Remove cards from the hopper.

## 6-9. Operational Tests-Variable Voltage and Frequency

a. Preliminary Procedure. Position the switches on the test set as follows.

115 VAC circuit breaker to ON
CANCEL to OFF
SYNC FAIL to OFF
EOM to OFF
SELECT to ON
SINGLE CARD/REPEAT to REPEAT
COMPARATOR INPUT rotary switch to DATA IN
ASSIGNED/NOT ASSIGNED to ASSIGNED COMPARATOR IN/OUT to OUT
AUTO/MAN to AUTO
b. Operation With Static Variations of Frequencies and Voltages.
(1) Position variable frequency and voltage controls on CML 5000A to the first (132 VAC, 50 CPS) position indicated on the chart below (positions indicated by an ' $X$ ').

| Test Voltage (VAC) |  | Test Frequency (CPS) |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 47.5 | 50 | 52.6 | 67 | 60 | 63 |
| 132 ..................... |  | X |  |  | X |  |
| 120 ..................... | X | X | X | X | X | X |
| 96 |  | X |  |  | X |  |

(2) Load card stack 'F' in hopper.
(3) Set the test set COMPARATOR switch to IN.
(4) Press START switch on card reader.
(5) Press START switch on test set and start one-minute timer.
(6) Verify that the 108 white cards are read in one-minute maximum.
(7) Repeat steps (2) and (4) through (6) for all remaining settings of frequency and voltage as indicated by an ' $X$ ' in the chart of step (1).
c. Dynamic Variable Voltage at 50 Hertz (120 $V A C)$.
(1) Adjust the variable frequency And voltage source for 50 hertz and 120 VAC.
(2) Remove card stack 'F' and load stack ' $E$ ' in the hopper.
(3) Press the card reader START switch.
(4) Press the test set START switch and start the one-minute timer.
(5) Vary the OUPTPUT LEVEL adjust on the CML N5000A from a nominal 120 VAC to a minimum of 96 VAC , then to a maximum of 132 VAC , and then return to 120 VAC. This cycle should be completed in approximately 60 seconds.
(6) Verify that cards continue to feed while voltage is varied, and that all 108 white cards are read in one minute maximum.
(7) Press the card reader STOP switch at the end of the cycle.
d. Dynamic Variable Frequency at 120 VAC (50 Hertz).
(1) Reload card stack 'E' in hopper.
(2) Press the card reader and test set START switches in sequence, and start the one- minute timer.
(3) Vary the FREQUENCY CPS adjust on the CML N5000A from a nominal 50 CPS to a minimum 47.5 CPS, then to a maximum 52.5 CPS, and return to 50 CPS. This cycle should be completed in approximately 60 seconds.
(4) Verify that cards continue to feed while frequency is varied, and all 108 white cards are read within one minute.
(5) Press the card reader STOP switch at end of the cycle.
e. Dynamic Variable Frequency at 120 VAC (60 Hertz).
(1) Adjust the variable frequency and voltage source to 60 CPS and 120 VAC.
(2) Reload card stack ' $E$ ' in hopper.
(3) Press CR and test set START switches in sequence, and start one-minute timer.
(4) Vary the FREQUENCY CPS adjust on the CML N5000A from a nominal 60 CPS to a minimum of 57 CPS, then to a maximum of 63 CPS, and return to 60 CPS. This cycle should be completed in approximately 60 seconds.
(5) Verify that cards continue to feed while frequency is varied, and all 108 white cards are read within one minute.
(6) Press card reader STOP switch at end of cycle.
f. Dynamic Variable Voltage at 60 Hertz.
(1) Reload card stack 'E' in hopper.
(2) Adjust the variable frequency and voltage source for 60 CPS and 120 VAC.
(3) Press the CR and test set START switches in sequence, and start one-minute timer.
(4) Vary the OUTPUT LEVEL adjust on the CML N5000A from a nominal 120 VAC to a minimum of 96 VAC, then to a maximum of 132 VAC, the return to 120 VAC. This cycle should be completed in approximately 60 seconds.
(5) Verify that cards continue to feed while voltage is varied, and all 108 white cards are read within one minute.
(6) Press CR STOP switch at end of cycle.

## 6-10. Shutdown

a. Press AC POWER switch on card reader.
b. Position 115 VAC circuit breaker on test set to OFF.
c. Position the CML N5000A HIGH VOLTAGE switch to OFF; then place the POWER switch to OFF.
d. Remove connection between card reader and CML N5000A.
e. Remove connection between card reader and test set.


$10:-x_{0}$
․un : -


mism







aditional illustrations and wire list


axkleao

oisk-rwe

Figure 8-1. Military standard for color marking
8-1. Change 7


Figure 8-3. Card reader, interconnection schematic diagram.


Figure 8-4. Card reader, control panel schematic diagram..


Figure 8-5. Ac circuits, schematic diagram.
8-2.7/(8-2.8 Blank) Change 1


Figure 8-6. Dc circuits, schematic diagram
8-2.9/(8-2.10 Blank) Change 5


Change 1

## Figure 8-7 (1). Rectifier and voltage regulators, schematic diagram (part 1 of 3 parts.)



Figure 8-7 (2). Rectifier and voltage regulators, schematic diagram (part 2 of 3 parts.)


Figure 8-7 (3). Rectifier and voltage regulators, schematic diagram (part 3 of 3 parts.)
Change 1 8-2.15/(8-2.16 Blank)


Figure 8-8. Power supply PS1 sequence module A12, schematic diagram
Change 8 8-2.17 (8-2.18 Blank)


Figure 8-9. Card reader mechanism circuitry, schematic diagram.
Change 4 8-2.19/(8-2.20 blank)



Figure 8-11. PC card A3 (No. SM546659-001), schematic diagram.


| POWER INPUT PINS |  |  |  |
| :---: | :---: | :---: | :---: |
|  | $Z 1, Z 3$ | $24, Z 5$ | $Z 2$ |
| $G R D$ | 4 | 5 | 4 |
| $+4.5 V D C$ |  | 7 | 10 |
| +12 VDC | 12 | 11 | 12 |
| -12 VDC | 14 | 1 | 6 |

Figure 8-12.1. PC card A4 (A65223-001), schematic diagram.


| POWER INPUT PINS |  |  |
| :---: | :---: | :---: |
|  | 210 | $Z 1$ THRU 29 |
| +4.5 VDC | 6 | NOT USED |
| GRD | 1 | 7 |
| +12 VOC | NOT USED | 13 |
| -12 VOC | NOT USED | 1 |

Figure 8-12.2. PC card A5 (A65227-001), schematic diagram.

## NOTE:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).


Figure 8-12. PC card A4 (No. A65215-001), schematic diagram.


NOTES:

1. PARTLIL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBEA OR SUBASSEMBLY DESIGNATION (S)
2. UNLESS OTHERWISE SPECIFIED:
all resistance values are in ohms.

| POWER INPUT PINS |  |
| :---: | :---: |
|  | 21 |
| $+4.5 V D C$ | 6 |
| $G R O$ | 1 |



Figure 8-13. PC card A5 (No. A65205-001), schematic diagram.


Figure 8-14. PC card A6 (No. A52630-001), schematic diagram.
8-4.1/(8-4.2 Blank)


Figure 8-15. PC card A7 (No. A65145-001) schematic diagram
Change 1 8-4.3/(8-4.4 Blank)


Figure 8-16. PC card A8 (No. A52634-001), schematic diagram.


NOTE:


Figure 8-18. PC card A10 (No. A53721-001), schematic diagram.



NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH
NUMBER OR SUBASSEMBLY DESIGNATION (s).

Figure 8-20. PC card A12 (No. A53721-001), schematic diagram.


Figure 8-21. PC card A13 (No. A52662-001), schematic diagram





| power invut pins |  |
| :---: | :---: |
|  | 21 TrRU 228 |
| +4.5VOC | 6 |
| GRO | 1 |

NOTES:

1. PAPTIAL REEERENGE DESIGNATIONS ARE SHOWN; FOR COMPLETE:
 2. UEESES OHHEEWISE SPECIIED:




Figure 8-23. PC card A15 (No. A65153-001), schematic diagram


Figure 8-24. PC card A16 (No. A65141-001), schematic diagram.
Change 2 8-4.21/(8-4.22 blank)

TM 11－7440－215－15／NAVSHIPS 0967－LP－324－0020／TO 31W4－2G－31
TABLE 8－1 LOGIC ASSEMBLY A1 WIRE LIST

| FROM |  | TO | FROM | TO | FROM | TO | FROM | TO |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CON | －PIN | CCN－PIN | CUN－PIN | CON－PIN | CON－PIN | CCN－PIN | CON－PIN | CON－PIN |
|  | － | － | Juこ－T | J03－V |  |  | XAC4－12 | XA15－ y |
|  | － | － | 」Oこ－ | Je3－R |  |  | XAU4－13 | JO1－ X |
| 102 | $-2$ | $\times \mathrm{AO} 4-21$ | 小uこ－u | 103 － |  |  | XAC4－14 | 101－N |
| Jot | －N | $\times{ }^{\times A O 4-14}$ | フos－U | Jc3－S |  |  | XAOA－16 | $\times \times 16-\mathrm{P}$ |
| JO： | －R | $\times{ }^{\times A O} 4-E$ | 10こ－v | J03－T |  |  | XAO4－17 | JCi－21 |
| J01 | －T | $\times \mathrm{AO4-11}$ | 10：－V | j03－x |  |  | XAO4－18 | XA15－J |
| 101 | －$V$ | $\times 104-05$ | Joミ－w | 103－v | XAC1－01 | JC2－A | $\times \mathrm{X} \times 4-19$ | JCi－ 23 |
| 101 | － x | XAO4－13 | JoE－$x$ | $103-\vee$ | XAO1－01 | XAO4－C1 | $\times \mathrm{A}, 4-20$ | XA15－ H |
| 101 | － 2 | $\times \mathrm{AO4-09}$ | 」とこ－ | Jc3－01 | XAC1－OE | TEIA－02 | XAU4－22 | NCI－L |
| 101 | －01 | $\times$ XAOS－U | T $>^{10 j-2}$ | XA15－17 | xA01－02 | JC2－02 | XAC4－22 | XAO4－04 |
| J01 | －03 | XAOS－$V$ | －Joj－01 | J03－Y | xaci－03 | $\times 103-03$ | XA04－22 | XAIE－$X$ |
| 301 | －05 | XAOS－$\times$ | 10ミ－C1 | $103-C$ | ＞xact－04 | XA1S－L | XACA－23 | XA1E－18 |
| Jol | －07 | $\times \mathrm{AOS-20}$ | $10=-01$ | tela－os | XAO：－05 | JC4－W | XAOS－${ }^{\text {a }}$ | $\times 106-A$ |
| J心1 | －09 | $\times \mathrm{AOS-}$－ | 10こ－02 | JC3－A | $\times$ XC1－06 | 104 －W |  | TEIC－OI |
| Ju1 | －11 | $\times \mathrm{AOS-F}$ | 」C3－05 | XAOG－AA | XAO1－06 | $10_{4}$－T | $\times$ AOS－E | $\times$ POO－${ }^{\text {a }}$ |
| J01 | －13 | $\times \mathrm{AOS-H}$ | J03－07 | $\times A O E-21$ | $X^{X A O L-O S}$ | J04－T | xaOS－e | teic－oz |
| J01 | －15 | XAOS ${ }^{\text {P }}$ | 10こ－08 | $\times{ }^{\times 100-15}$ | $\times \times A O 1-10$ | 104－21 | $\times$ XOS－ C | XA1S－C |
| JO1 | $-17$ | $\times$ AUS－12 | $10=-09$ | $\times A \cup E-18$ | XAOL－12 | $104-Y$ | xaOS－C | $\times \mathrm{AOS-C}$ |
| J01 | －19 | $\times$ X $\times$－ 4 －07 | 」0こ－10 | $\times \mathrm{ACO}-17$ | XAC1－13 | J04－r | XAOS－C | XAO3－ C |
| JO1 | －21 |  | J0こ－ 11 | $\times$ X ${ }^{\text {P }}$（ $06-14$ | $\times$ AC 1－14 | $\times$ 116－07 | $\times$ AOS－${ }^{\text {d }}$ | Jer－09 |
| Jol | －23 | XAO4－19 | Jo＝-12 | XAO6－13 |  |  | XACS－E | XA13-11 |
| J02 | －${ }^{\text {a }}$ | $\times \mathrm{AOL-01}$ | J0こ－13 | XAO6－12 |  |  | XAOS－${ }^{\text {P }}$ | J01－11 |
| 102 | －C | $\times \mathrm{AOL}-\mathrm{C}$ | 103－14 | XAC6－10 |  |  | XAOS－H | J01－13 |
| J02 | $-c$ | JC2－04 | J0ミ－15 | XAUG－04 |  |  | XAO5－J | j01－15 |
| J02 | －$F$ | $\times{ }^{\times 116-08}$ | JuE－ 16 | XAOE－05 | XA01－20 | XA10－12 | XAOS－K | XA13－06 |
| JO2 | －H | $\times \mathrm{A16-03}$ | Jこ | XAOG－L |  |  | xaUS－L | $\times$＋13－M |
| J02 | －J | $\times$ A1O－AA | JuJ－18 | XAO6－ 5 | $\times A O 1-22$ | XAOS－ 0 | XAOS－u | Jot－01 |
| J02 | －k | XAl o－L | $\cdots ¢=-29$ | XAOO－15 | ＋ |  | xaUS－v | J01－03 |
| J02 | －L | XA16－09 | Joi－ 20 | XAOE－D | XACJ－$C$ | xaus－C | XAOS－ | XA13－03 |
| J02 | －m | XAl G－ N | Joj－21 | XA15－M | $\times$ AOE－E | XA16－14 | XAOE－$\times$ | 101－05 |
| 102 | －N | $\times \mathrm{AlO}-20$ | J0ミ－22 | XA1 S－0 ${ }^{\text {P }}$ | XAOS－F |  | XAOS－Y | XA13－C |
| Jö | －V | $\times$ AO3－22 | Ju4－T | $\times$ XAOL－09 | XAUZ－H | $\times$ A1 $5-05$ | XACS－$Z$ | $\times$＋ 13 3－08 |
| J02 | － |  | Je4－T | XAO1－08 | XAOE－J | XA15－09 | xaOS－ci | $\times 106-01$ |
| J02 | － x | XAl ${ }^{\text {P }}$－$Y$ | 104 － | XAO1－06 | XAO3－ K | XA16－21 | XAOS－01 | TEIC－01 |
| Juc | －0： | XAOI－${ }^{\text {a }}$ | 104 －w | XAO1－05 | XAOE－P | J02－06 | XA05－02 | reic－az |
| Jca | －02 | ×A01－02 | J04－r | $\times \mathrm{AOR1-23}$ | XAOE－S | J02－07 | $\times A 0 \leq-03$ | $\times$＋06－03 |
| 102 | －04 | J02－C | 1 $304-r$ | $\times \mathrm{AOL-12}$ | $\times A C E-T$ | J02－15 | XAOS－C3 | X $\times$（04－03 |
| 102 | －0t | $\times \mathrm{OSB}-\mathrm{P}$ | － $104-10$ | J04－19 | $\times$ AOE－U | J02－16 | XA05－07 | X ${ }^{1} 13$ 3－A ${ }^{\text {a }}$ |
| J02 | －07 |  | Jc4－19 | JC4－16 | XAOE－ | 102－21 | XAC5－10 | XAO4－06 |
| Jue | －0¢ | $\times 103-05$ | 104－19 | JC4－21 | XACE－ | Józ－17 | XAOS－10 | $X A 15-X$ |
| Juz | －0s | $\times 103$－ Y | 104－21 | XAO1－10 | $\times$ ACE－$\times$ | JC2－20 | $\times \times$ O－11 | XAOS－13 |
| J02 | －10 | XA03－09 | ＞ $104-21$ | J04－19 | XAOE－Y | － $\mathrm{C2}$－09 | $\times A O E-12$ | $\cdots{ }^{\text {C1－17 }}$ |
| J0\％ | $-14$ | × $\times 103-02$ |  | －03－01 | X $\times 10 \leq-01$ | JC2－14 | XAOE－13 | XAOS－11 |
| 」○こ | －15 | xau3－${ }^{\text {x }}$ | TE1A－01 | $\times \times 101-A$ | PXAC3－03 | $\times$－${ }^{\text {J }}$ 4－03 | $\times A O E-14$ | $\times$（14－U |
| 102 | $-1 t$ | $\times \mathrm{xAOS}-U$ | tola－02 | XAO1－02 | XAOE－03 | $\times \mathrm{AO} 1-03$ | $\times \mathrm{AO}=-20$ | دC1－07 |
| J02 | －17 | xaOS－w | 1日1A－02 | $\times \times 101-\mathrm{B}$ | XACE－05 | J02－08 | $\times{ }^{\text {P }} 0 \leq-21$ | XA1 3 －07 |
| 」0こ： | －18 | $\times \mathrm{AOS} 3-\mathrm{x}$ | tele－ul | $\times{ }^{\text {X }}$－4－Cl | XAC $=-06$ | JC2－19 | XAOE－A | XaUS－a |
| J0く | －19 | x 103－06 | THIE－O1 | XAU4－F | $\times A O=-07$ | J02－20 | $\times \mathrm{ADE}$－B |  |
| 102 | －20 |  | TEIE－02 | XAO4－02 | XAOE－OE | J0\％－22 | XACE－D | J03－20 |
| Ju2 | －21 | $\times \mathrm{AOS}$－ V | TE1E－02 | XAO4－${ }^{\text {－}}$ | $\times{ }^{\times C J}-09$ | J0＜－10 | XAOC－$E$ | XAOT－L |
| 102 | －22 | $\times 103-08$ | teac－01 | XA05－01 | XACE－13 | XA16－12 | XAOE－F | XAOT－${ }^{\text {d }}$ |
| J03 | －A | JC3－C | t日ac－01 | XAOS－A | XAO $=15$ | XA16－H | XAOE－L | Jc3－17 |
| J0ミ | －A | J03－02 | TE1C－02 | $\times \times 105-02$ | $\times A O E-16$ | XA1S－AA | XaUe－M | $\times \mathrm{AOT-K}$ |
| 103 | －A | 203－0 | 181c－02 | $\times 405-8$ | $X A O E-17$ | XA15－12 | xade－${ }^{\text {N }}$ | $\times$－ $07-21$ |
| 10ミ | － B | J03－0 | TEIC－O1 | XAO7－01 | XAC ${ }^{\text {P }}$－18 | XA14－${ }^{\text {W }}$ | XACE－P | XA14－10 |
| 103 | －c | $J 03-A$ | TEdc－01 | $\times{ }^{\times A O T-A}$ | $\times A C E-19$ | XA14－2 | XACE－ 5 | 103－18 |
| 」uう | －C | J03－01 | 1615－02 | XA07－02 | XAC $=-20$ | XA15－18 | xave－${ }^{\text {a }}$ | X A $_{1} 4-17$ |
| JoE | － 0 | 103 －B | rilo－02 | xAOT－${ }^{\text {P }}$ | XACE－21 | XA1C－E | XACE－U | X A $14-11^{\text {4－}}$ |
| 102 | －D | 103 －A | T 01 E－01 | XA10－01 | XAUE－22 | JUz－v | XACC－V | $\times$ XOT－V |
| J03 | －F | J03－K | tese－0i | XAOS A | XAU4－${ }^{\text {a }}$ | XAU4－F | XAOE－ | XAOT－F |
| jo3 | －F | J03－J | tele－02 | $\times \mathrm{A}, 0-\mathrm{B}$ | XAC4－${ }^{\text {P }}$ | TEIE－O2 | XAOE－$\times$ | $\times$ x ${ }^{\text {P－}} \mathrm{H}$ |
| J03 | －H | Jc． 3 －K | 161F－01 | XA12－01 | $>^{\times A G A-C}$ | XAOL－C | XAOE－AA | JC3－05 |
| J03 | $-\mathrm{H}$ | $\times \mathrm{OL}-\mathrm{B}$ | Tolf－01 | XA11－A | Pxaca－$C$ | $\times 105-\mathrm{C}$ | $\times A C E-C 1$ | XAOS－01 |
| J03 | －J | J03－L | telf－02 | XA11－ $\mathrm{E}^{\text {a }}$ | XACA－D | XA16－C | XACE－02 | XA，S－R |
| $10=$ | －J | J03－f | Tolc－01 | XA1 3－01 | $\lambda A C 4-E$ | J01－R | $\times A O \in-C \geq$ | XAUS－03 |
| 103 | －k | J03－M | TbIG－01 | XA13－A | XAU4－F | T615－01 | XADE－O3 |  |
| Joj | －K | $103-\mathrm{H}$ | TEIE－0¢ | XA13－02 | XAC4－F | XAOA－${ }^{\text {a }}$ | XADE－04 | Jc3－15 |
| 203 | － x | J03－F | rele－02 |  | XAC4－02 | TEAB－OI | XAOE－OS | 103－16 |
| J0\％ | － 1 | JC3－J | TEIHOCOL | XA15－ $\mathrm{UA}_{1}$ | XAC4－01 | xAOL－01 | XAOE－OE | XAO7－E |
| J03 | － 1 | J03－N | 701H01 | XAIS－A | XAC4－C2 | TB1E－02 | XACE－ 10 | JC3－14 |
| J0ミ | －m | JC3－K | TEIHT02 | $\times A_{15} 502$ | $\times$ AC4－U | $\times$ ¢03－03 | XACt－11 | XAUT－AA |
| コにこ | －M | J03－p | － $\mathrm{T}^{\text {T }} 1 \mathrm{H}-02$ | XA15－8 | XAC4－03 | XAOS－03 | XAOE－1a | J03－13 |
| J03 | － N | Jos－R | －xaUl－a | TEIA－01 | XAC4－04 | $\times \mathrm{AO} 4-22$ | $\times \mathrm{AOE}-23$ | Jc3－12 |
| Joミ | － N | J03－L | XACi－ 2 | Jca－01 | XACA－05 | JOL－V | XACE－14 | JC3－11 |
| Joき | －P | $103-5$ | XACI－${ }^{\text {P }}$ | Jc3－H | XAC4－06 | $\times$ XOS－10 | XACE－1 $=$ | J03－19 |
| 103 | －P | dc3－M | XAO 1－ e | TG1A－02 | $\times$ XAC－4－07 | JC1－19 | XAUE－16 | $\times 107-$ W |
| 103 | $-\mathrm{F}$ | J03－N | ＞$\times$ AC：-C | $\times 104-\mathrm{C}$ | XAC4－OE | xals－2i | XAOE－17 | J03－10 |
| J0\％ | － H | J03－1 | P $x$ ACL－$C$ | J02－C | XA04－09 | JCi－ 2 | XADE－18 | J03－09 |
| J0こ－ | － s | $103-\mathrm{P}$ | －xaOL－ 0 | XA15－N | XAO4－10 | XA15－14 | $\times A O \in-19$ | Ju3－08 |
| J03 | －s | $103-u$ | － |  | XAV4－11 | J01－T | XACE－20 | $\times{ }^{\text {A }}$－ 7 |

TABLE 8－1 LOGIC ASSEMBLY A1 WIRE LIST

| FROM | TO | FROM | TO | FROM | TO | FROM | TO |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CON－PIN | ccn－pin | CCA－P1N | cin－Pin | CCN－PIn | cun－pin | CCN－FIN | con－pin |
|  | J03－67 | xacis－19 | $x \triangle O S-A A$ | XA $1 C-1$ | XAOQ－ | XA11－15 | XA12－06 |
| XAOt 22 | XRUT－ N | $\times 408-20$ | XAUS－ | XA1C－M | XAJS－R | XA11－16 | $\times$ A．O－19 |
| XACE－＜3 | XA14－12 | xacer 21 |  | XA：C－N | XAS2－ N | XA1：17 ${ }^{\text {P }}$ | xA12－05 |
| XAUT－${ }^{\text {a }}$ |  | $\times A C E-22$ | XAUT－04 | $X A \perp C-P$ | XAOS－10 | $X_{A} 11-18$ | $\times A_{1} 2-C$ |
| XACT－${ }^{\text {a }}$ | TEIE－OI | XACE－23 | XAO7－08 | XAIC－R | XAOS－$C$ | XA12－1S | $\times{ }^{+12-E}$ |
| XAUT－${ }^{\text {P }}$ | $\times 108-\mathrm{B}$ | XACS－A | XAIO－A | XAAC－$S$ | XAO9－02 | $\lambda_{A 1} 11-20$ |  |
| $\times$ ¢CFI－ | YEID－U2 | XaOS－A | rele－ui | XAIC－T | XA12－${ }^{\text {P }}$ | XA11－2： | XAI2－$\times$ |
| $\times$ AOT－D | XAlA－C | XACS－B | $\times \mathrm{AlO-B}$ | $X A \perp C-U$ | XA11－06 | XA11－＜2 | Xaut－E |
| XAU7－${ }^{\text {P }}$ | XAUG－F | XACS－C | XA10－${ }^{\text {P }}$ |  |  | XA11－23 | x 209 －23 |
| XALT－E | XA14－F | XaUs－ 0 | XASC－OS | XA： $0-\mathrm{V}$ | xa09－16 | XALE－${ }^{\text {a }}$ | XA11－A |
| XAC7－E | xave－08 | XACS－ 0 | $\times$ P01－22 | XA：C－${ }^{\text {W }}$ | XA13－H | XA12－E | XA11－${ }^{\text {P }}$ |
| XAと7－F | XA：A－U4 | XACS－E | $\times{ }^{\text {P }} 11-E$ | XA1C－ | $\times \mathrm{AOP-}$ | $\times \mathrm{A} 12=0$ | XA11－18 |
| $\times 407-F$ |  | XACS－E | XAOS－03 | XAPC－${ }^{\text {P }}$ | $\times A_{1}{ }^{\prime}-R$ | $\times$ ¢12－0 | XA11－${ }^{\text {P }}$ |
| XACJ－ H | xave－$\times$ | XAGS－F | $\times$ A11－F | XAPC－ 2 | $\times 409-08$ | xa12－E | XA11－19 |
| XAC7－ H | XA14－05 | xaOS－F | $\times A O E-12$ | $\times A \perp O-A A$ | XA09－20 | XA」こ－F | XA11－20 |
| XAC7－K | XA14－E | XMOS－ H | XA12－p | $\times \mathrm{A} \perp 1-01$ | Tole－01 | $\times 412-\mathrm{H}$ | XA1O－M |
| XAOT－K | $\times A O B-M$ | XAUS－$J$ | XA12－04 | XA1 $C-\dot{C}$ | XA12－v2 | X41z－ H | XA13－Y |
| $X A C 7-2$ | XAIS－${ }^{\text {d }}$ | XACO－K | $x$ A1z－S | $\times \mathrm{A} 1 \mathrm{C-O}$ | XA13－17 | XA12－J | XA1O－J |
| $\times A C 7-L$ | $\times \mathrm{AOG}$－E | XAUS－L | $X \mathrm{AlO-X}$ | XA $10-04$ | $\times \mathrm{AOS-} 2$ | $\times$ A12－ | $\times \mathrm{Al} 3-\mathrm{X}$ |
| XACT－ N | $\times \mathrm{Al} 4-\mathrm{m}$ | XAC9－m | XA12－08 | XA 1 C－CE | XAOS－D | XA： 2 －K | XA11－21 |
| XAC7－ N | $\times A O E-22$ |  |  | XA $1 C-0 E$ | $\times$－09－C3 | XA」 ${ }^{\text {¢ }}$－ | XA11－Y |
| XAU7－P | X A $14-03 ~_{\text {4，}}$ | XACg－ N | $\times$ A12－13 |  |  | $\times A_{12-M}$ | XA11－ C |
| XAUT－${ }^{\text {P }}$ |  |  |  | $x A: C-U T$ | XA09－06 | XAIE－$N$ | XA13－＊ |
| XAC7－T | XA16－06 | XACP－${ }^{\text {P }}$ | XA」 $G-18$ | $x A \perp C-\cup Z$ | $\times 409-07$ | $\times \mathrm{Al}=-\mathrm{N}$ | XA1O－${ }^{\text {N }}$ |
| XACT－U | XA14－19 | XAOQ－${ }^{\text {P }}$ | $\times \mathrm{AlO-m}$ | XA 1 C－ט9 | XAOS－Y |  | XAOS－ H |
| XACT－$V$ | XA14－K | XACg－S | XA12－16 | $X_{A}: C-10$ | XAOQ－21 | XA12－R | XAOS－04 |
| XAUT－ | xave－$V$ | XAC9－T | $x$ x $\cup 8-13$ | $x^{\prime} 1_{1} 0-11$ | $\times$ A09－15 | $X A 12-5$ | $\times \mathrm{AOS-K}$ |
| XAC．7－W | $\times{ }^{\times 14} 4{ }^{-1}$ | XAC9－T | XA1： | XA： $0-12$ | XA11－03 | XA1 $=$ | XA13－V |
| XAO7－W | XAOO－16 | XACO－U | XA11－U | XA10－12 | XAUl－20 |  | XAIO－ Y |
| XAC7－$\times$ | XA14－13 | XACS－ U | xave－J | $\times A_{1} 0-13$ | $\times{ }^{\times 11-L}$ | XAIz－$V$ | $x$ A12－13 |
| xACi－ r | XA：4－22 | $\times \mathrm{ACO}$ | XA10－1 | $\times 410-14$ | XA13－18 | XA1E－$V$ | XA11－ 5 |
| XAUT－AA | XA14－J | $\times \mathrm{AC9}$－ |  | XA1C－15 | XA13－19 | XA1z－W | $\times A_{1} 3-\mathrm{P}$ |
| XAC7－AA | $\times 100-11$ | $X A C O-X$ | XA11－$\times$ | $X A \perp C-16$ | XAOS－09 | XA1 $2-X$ | XA11－K |
| XA07－01 | xa0b－01 | XAC9－$\times$ | XAOS－14 | $x A \perp C-17$ | XAOS－14 | XA12－Y | XA11－04 |
| XA07－C1 |  | XAC9－ Y | XA10－09 | $\times A: C-18$ | XAOS－P | XAİ－ | XA1：－05 |
| $\times \mathrm{AOT-02}$ | teid－02 | XAC9－ 2 | $\times$＋110－04 | $x_{A} 16-19$ | $X^{\text {A }} 111-16$ | $X A_{1} 2-A A$ | XA11－02 |
| xa07－02 | xave－uz | $\times A C 9-A N$ | XAOE－19 | $\times A 1 C-20$ | XA12－20 | $x_{A 1}=1-02$ | TEIF－OI |
| XAO7－04 | $\times 108-22$ | xacs－0： | XA11－01 | －$\times 1 \times 10-21$ | xati－ 2 | $\times A_{1} \hat{z}-02$ | XA13－0 ${ }^{\text {P }}$ |
| XACT－0S | $\times A \cup S-A A$ | XAC9－01 | XAUE－$\quad$（ | －xalo－＜2 | XA11－p | $x_{A} 12$－02 | $\times 410-02$ |
| $\times \mathrm{AOT-OC}$ | xaOE－${ }^{\text {a }}$ | xacs－u2 | XAJ $0-5$ | $\times A_{1} 1-23$ | XA1 $2 \sim 3$ | XA1 $=03$ | $\times$ A13－13 |
| $\times$－ $07-07$ | xaOb－ K |  |  | $\times A_{11-A}$ | $\times{ }^{\text {P1 }} 2-\mathrm{A}$ | －XA1z－04 | $\times$ AOO－J |
| $\times 407-08$ | xave－23 | XAC5－us | XA10－5 | $\times \mathrm{A} 11-\mathrm{A}$ | relt－oi | XA1 ${ }^{\text {－}}$－US | XA11－17 |
| XACT－CS | $\times{ }^{\times O O-17}$ | XACS－04 | XA12－R | XA11－ | $\times{ }^{\text {¢ }}$ 2－ 8 | －Xa，${ }^{\text {a }}$－00 | $\times$ A $^{\text {1－1－15 }}$ |
| XAC7－30 | XAOU－ N | $X A C 5-05$ | XA12－09 | $\times \mathrm{A} 11-\mathrm{B}$ | telf－oc | XA12－07 | $\times$ A1－$^{\times}$ |
| XAC ${ }^{\text {Patic }}$ | XAOE－M |  |  | XA11－C | XA12－m | XA $12-08$ | $\times$ atos－M |
| XAC 7－17 | $\times \mathrm{AOE}-\mathrm{X}$ | xacs－06 | $\times$ A $10-07$ | －XA11－0 | XA12－07 |  | $\times \mathrm{COS}$－0： 2 |
| XAC7－1E | x $\times 005-21$ |  |  | －XA $11-\mathrm{E}$ | XAOS－E | XA $1=10$ | XAOS－18 |
| $\times{ }^{\text {A O }}$－ $7-19$ | $\times$ XAOS－ 1 | XACS－07 | $\times$ A10－08 | XA11－F | $\times \mathrm{AOS}-\mathrm{F}$ | XA12－11 | $\times \mathrm{AO9-15}$ |
| $\times$ ¢07－2C | XAOB－16 |  |  | XA1： H | XA12－19 | XA12－12 | $\times{ }^{\times A 11-N}$ |
| $\times \mathrm{COT-22}$ | XAl4－ H | XACS－Ct | $\times A_{10-z}$ | $\times A_{1}$－${ }^{\text {d }}$ | $\times \mathrm{AlO-}$ | －$X^{\prime} 1212-13$ | $\times$ AO9－ N |
| $\times \mathrm{A} 07-21$ | $\times \mathrm{AOG}-\mathrm{N}$ | XACS－0y | XA10－16 | XA11－K | XAI $2-x$ | $\times A_{1}=14$ | XA13－10 |
| $\times A O E-A$ | $\times 407-\mathrm{A}$ | XACS－10 | XAI $0-P$ | XA11－L | XA1 $0-13$ | $\times{ }^{+1} 12-15$ | XA13－R |
| XACE－${ }^{\text {a }}$ | XAUT－ 6 | XACS－11 | XAOE－11 | －XAI $1-\mathrm{m}$ | $\times$ ATO－C | XA12－16 | $\times \mathrm{AOS-S}$ |
| XAOE－E | XA11－22 | XAOS－12 | XA11－12 | －XA11－N | $\times$－ $12-12$ | $\times A_{1}=17$ | $\times$ AOS－17 |
| XAOE－F | XA14－20 | XACS－12 | XAOS－$V$ | －XA11－P | XA10－22 | $\times A_{1}=-18$ | $\times A^{11-14}$ |
| XACE－ H | $\times{ }^{\times 107-00}$ | $\times A O \leq-13$ | $\times{ }^{1} 10-K$ | －XAL1－${ }^{\text {a }}$ | $\times$ A1C－Y | XA1 $=-19$ | XA11－M |
| XACE－J |  | XAOS－14 | XA10－17 | XA：1－ 5 | XAl $2-V$ | XA12－20 | $\times{ }^{\text {x }}$（3－L |
| XAOE－K | $\times \mathrm{AOT-07}$ |  |  | XA11－${ }^{\text {P }}$ | XAOS－$T$ | XA1E－20 | $\times$－ $210-20$ |
| XACE－L | ＋A07－19 | －xaus－12 | $\times$ A10－11 | XA1 $1-U$ | xaOS－U | XA1 $=21$ | XA1t－09 |
| XAOE－M | $\times \mathrm{AO} 7-16$ | $x A O S-1 \epsilon$ | $\times \mathrm{x} 10-\mathrm{V}$ | $\times A 11-\mathrm{V}$ | XA：2－D | XA18－22 | X $A_{1} 11-10$ |
| XACE－ N | $\times$－ $07-15$ | XAOS－17 | XA12－17 | XA11－${ }^{\text {W }}$ | $\times \mathrm{AOB}-10$ | XA12－23 | XA13－K |
| XAOE－ H | xAOS－23 | XACS－18 | XA12－10 | XA11－$X$ | xaOS－$\times$ | $\times A_{1}=23$ | XA10－23 |
| XACEV | $\times A D S-12$ | XACS－19 | XA12－11 | XA1 1－$Y$ | XA12－ | 入A1E－${ }^{\text {A }}$ | XA13－F |
| XACE－${ }^{\text {a }}$ | $\times$ X 0901 | －XAOS－2C | $\times$ A1O－AA | －XA11－ 2 | $\times$－${ }^{\text {P－21 }}$ | $\times A_{1}=-\mathrm{A}$ | TE1年01 |
| XACL $\times$ | XAOT－17 | xacs－21 | $\times \mathrm{Alc} 10$ | －$\times$ A11－AA | $\times \triangle \cup E-09$ | $x^{+11}=-2$ | XAI4－E |
| XAOE－AA | $\times \mathrm{AO} 7-05$ | $\times \mathrm{AOS}-22$ | $\times \mathrm{AOC-18}$ | XA11－01 | xaOs－01 | $\times A_{1}=-8$ | TE1G－02 |
| XAOE－OL | XAOT－01 | XACS－23 | xA11－23 | XA11－C2 | XA12－AA | $x A_{1}=-C$ | XAOS－Y |
| － XACE －02 | $\times \mathrm{AUT-02}$ | XA $C \leq-23$ | XAUE－K | XA1 $1-03$ |  | $X A_{1}=-E$ | XA1A－ 21 |
| XACE－03 | XAOS－E | $X A \perp C-A$ | XAOS－${ }^{\text {a }}$ | XA11－04 | XA12－Y | XA1EーF | XA13－${ }^{\text {a }}$ |
| $)^{\text {XACE }}$－ 05 | $\times$ A08－01 | $\times A 1 C-2$ | $\times \mathrm{OS}$－ B | $\times A \leq 1-0 \leq$ | XA12－z | $\times A^{\prime}=-F$ | $\times \mathrm{A1O-N}$ |
| －$A$ AOE－07 | XA11－11 | $\times \mathrm{A} 1 \mathrm{C}-\mathrm{e}$ | TとIE－02 | －XA， 1 －0t | $\times{ }^{\text {P1O－U }}$ | XAIE－H | $\times \mathrm{AlO}$－ |
| XACE－09 | XA11－AA | $\times A 10-C$ | $\times A_{1} 11-M$ | $x x_{11-c 7}$ | $\times A: O-F$ |  | $\times 208-06$ |
| XACE－10 | XA11－${ }^{\text {P }}$ |  |  | XA11－08 | $\times A_{1} 0-E$ |  |  |
| XACE－11 | $\times$ AOS－11 | XAIC－ 0 | XA11－J |  |  | XA1 $=$－ x | XA1 2－23 |
| XAOE－12 | xaOS－F | XAIC－E | $\times A_{11-08}$ | XA11－C9 | xA12－21 | $X A_{1} E-L$ | $\times{ }^{\times 112-20}$ |
| XACE－13 | $\times$ MOS－ 1 | XA：C－F | $\times A_{1} 1-07$ | XA11－10 | XA12－22 | XA1 $=-\mathrm{m}$ | XAUS－L |
| XACE－14 | XAOS－$x$ |  |  | X $\mathrm{A}_{1} 11-11$ | $\times \mathrm{AOEEO}$ | XAIE－N | $\times{ }^{\times A 13-5}$ |
| XAOE－10 |  |  | XAIz－${ }^{\text {ch }}$ | XA1）－12 | $\times \mathrm{COS}-13$ | －XA1 | $\times A 13-F$ |
| XAVE－17 | $\times \mathrm{AOT-09}$ | XA：$C$－${ }^{\text {，}}$ | XA1 2－J | XA1：1－13 | XA12－U | －XA1 | XA12－${ }^{\text {W }}$ |
| XACE－18 | $\times$ AOS－22 | XA1C－K | XAUS－1S | － A1）$^{\text {a }} 14$ | XA12－10 | $X A 1 \Xi-R$ | XA12－15 |
| ［ $\times$ AOB－0； | $\times$－08－05 |  |  |  |  |  |  |

TABLE 8－1 LOGIC ASSEMBLY A1 WIRE LIST

| FROM | TO | FROM | TO | FROM | TO |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ． CN －PIN | CON－PIN | CON－PIN | CON－PIN | CON－PIN | CON－PIN |
| M $A_{1}=-\mathrm{s}$ | XA1 J－${ }^{\text {P }}$ | XA15－J | X ${ }^{\text {（ }}$－4－18 | XA1te－21 | xau3－K |
| $X A_{1}=-5$ | XALJ－$N$ | $X A_{1} \leqslant k$ | XA14－P | $\times \mathrm{A}$ 1e－2z | XA15－AA |
| XAIE－T | XA13－14 | XA1E－K | XA16－19 | E 1 | Joi－AA |
| XA1 | XA14－01 | XA15－1 | XAO1－0．4 | E | T日2－7日 |
| AIE－U | XA14－A | XAIE－M | XA1E－15 | E2 | －02－AA |
| A 1 E－U | XA13－${ }^{\text {S }}$ | XA15－M | 103－21 | E 3 | JO3－AA |
| $\times$－ | XA12－${ }^{\text {P }}$ | XA1E－$N$ | XAOL－ |  |  |
| XAL $=$－W | XA12－N | XA1E－$N$ | XA15－ | Jo：－AA Jo2－AA | E ${ }^{\text {e }}$ |
| XA1E－$x^{\prime}$ | XAİ－J | XA1E－ P | XA16－13 | J03－AA | E 3 |
| XA1E－ | XA12－H | $\mathrm{X} \cdot 1.15 \mathrm{R}$ | XAU6－02 | Joa－AA | $\varepsilon 4$ |
| $X A_{1}=-A A$ | xaus－07 | XAIE－U | $\times A L G-M$ | St－C | TE1－J1 |
| XA1 $=-01$ | XA13－12 | XA15－ | XA1G－$V$ | SI－N．O． | $\times$－16－10 |
| $\times A_{1}=-01$ | teig－us | KA1E－ | XAiS－${ }^{\text {N }}$ | TBP－J1 | St－c |
| $\times A_{1}=-02$ | XA14－02 | $x A_{1} \leq-x$ | $\times \times 16-\mathrm{D}$ | TE：－01 | TE3－1旦 |
| XA $1=-02$ | TG1G－02 | XA1E－$X$ | XAU5－10 | TB1－02 TB2－18 | TE3－2B $\times$ AOI－C |
| XAI $=-03$ | XAOE－W | $X A 15-Y$ | $\times$ XO4－12 | TB2－18 T $82-1 \mathrm{~B}$ | ＋AOS－C |
| XAI $=-65$ | XAIA－AA | $\times A 15-A A$ | xAU3－16 | TB2－2B | $\times$＋AO1－03 |
| xalこ－co | $\times$ AUS－K | XAIE－AA | $\times$ A1t－22 | T日大－38 |  |
| $\times A_{1}=-07$ | XAO5－21 | $X_{A} 1 \leq-C^{\prime}$ | XA16－01 | TB2－48 | $\times$ AOS－OE |
| $x A 15-08$ | XAU5－2 | XA1退－01 | TE1H－01 | TB2－5B | $\times$ A03－A |
| $\times \times 1=-09$ | XAIC－02 | XA $1 \leq-02$ | TEIH－02 | T62－78 | E 1 |
| XAI $=-10$ | XA）2－14 | X ${ }^{1} 15-02$ | $\times 416-02$ | TE3－1B | T81－01 |
| XA13－11 | XAUS－E | XA15－03 | XAUS－03 | TE3－2日 $\times A O L-C$ | TB1－02 TB2－1日 |
| XA：$=-12$ | xat 3－01 | X $A_{1} \leq-05$ | $\times \mathrm{AOS}$－ H | $\begin{aligned} & \times A D:-C \\ & \times A O 1-O B \end{aligned}$ | TB2－28 |
| XAIE－12 | XA13－14 | $\times{ }^{(1)} 5-07$ | $\times \mathrm{Al} 4-\mathrm{N}$ | XAO1－09 | T日2－4日 |
| XA $1=-13$ | XA12－03 | $X A 1 \leq-08$ | J03－22 |  | T $82-3 \mathrm{~B}$ |
| XA $15-14$ | Xal3－T | XA15－09 | $\times 103-J$ | $\times$－${ }^{\text {P3－}}$ A | T日2－5日 |
| XA $1=-14$ | xal3－12 | XA $15-10$ | $\times \mathrm{AlO}$－W | ×a03－01 | TB2－5日 |
|  |  | X $A 1 \leq-11$ | XA16－17 | $\times \mathrm{AOA}-\mathrm{C}$ | TB2－1B |
| XA1 $=18$ | XA1 14 | XA1E－11 | XA14－15 | $\times \mathrm{COS-OE}$ | XA13－J |
| XA1 $=19$ | XA10－15 | $x_{4} 1 \leq-12$ | $\times$（AOJ－17 | XA16－10 | S1－N．O． |
| XA14－ 4 | XA13－U | XA1E－13 | $\times{ }^{\text {P }} 16-04$ |  |  |
|  | XA13－6 | XA $15-14$ | XAU4－10 |  |  |
| XA14－$C$ |  | $\times 415-15$ | XA14－23 |  |  |
| XA14－0 |  | XA15－16 |  |  |  |
| CA1A－E | XAOT－K | XALE－17 | 103－2 |  |  |
| A1a－F | $\times 207-E$ | $\times A 1 \leq-16$ | $\times$（AOJ－20 |  |  |
| A14－H | $\times$ ¢ 0 7－？ 1 | $\times(1 \pm-15$ | $\times \mathrm{AlG-F}$ |  |  |
|  | $\times$ PU ${ }^{\text {P－AA }}$ | X $A_{1} \leq-20$ | $\times 116-06$ |  |  |
| XA14－K | xa07－V | $X A_{1}$ S－21 | $\times \mathrm{AO} 4-08$ |  |  |
| XA， 4 － L | XAUT－ | XA $1 \leq-23$ | XAL4－U |  |  |
| XA14－M | $\times \mathrm{AOT-N}$ | $\times A 1 E-A$ | XA15－A |  |  |
| XA14－ N | $\times$ A15－07 | XA1E－${ }^{\text {P }}$ | XA15－B |  |  |
| $\times A 14-\mathrm{F}$ | xal 5 －K | XA：$E$－$C$ | X $\mathrm{AOM}^{\text {－}} \mathrm{D}$ |  |  |
| $\times A_{14-}{ }^{\text {a }}$ | $\times$ AOS－14 | XA1E－ 0 | Xals－${ }^{\text {x }}$ |  |  |
| $X A 14-U$ | XA15－23 | XA1E E |  |  |  |
| XA14－ | $\times \mathrm{A}, 3$－1e | XA1t－F | XA15－19 |  |  |
| $\times$ ¢ 14 － | $\times{ }^{\times 15} 5$－ | XAIE－is | $\times$ AOB－15 |  |  |
| $x \rightarrow 1-2$ | XA15－F | XA1t－J | XAIE－H |  |  |
| $X{ }^{\prime} \times 14-2$ | $\times$ AU3－14 | XA1t－K | XA1 ${ }^{\text {P }}$－J |  |  |
| XA14－AA | xA13－us | XAIE－ | Juz－K |  |  |
| XA14－01 | xal3－T | XA1E－M | MAIS－U |  |  |
| XA $14-02$ | $x x^{\text {x }}$ 3－02 | KA1E－N | J02－m |  |  |
| $\times \mathrm{A} 14-03$ | x吅 7 －P | $\times \mathrm{A} 18-\mathrm{P}$ | $\times \mathrm{AO} 4-16$ |  |  |
| XA 14－G4 | $\times \mathrm{AOT}$－F | XA：$t-\mathrm{V}$ | XA15－ |  |  |
| $\times \mathrm{A}, 4-05$ | XA，7－${ }^{\text {P }}$ | XAIC－ | xals－10 |  |  |
| XA14－00 | $x A 10-05$ | XAI -X | $\times 104-22$ |  |  |
| xal4－10 | MAOS－P | XAIt－ Y | J02－ x |  |  |
| XA14－11 | xa06－${ }^{1}$ | XAIt－$Z$ | Jca－w |  |  |
| XA14－12 | $x \times 06-23$ | $\times A \cap C-A A$ | J02－J |  |  |
| XA14－13 | $\times 107-\times$ | $\times$ A1E－O2 | $\times 115-01$ |  |  |
| XA14－15 | XA15－11 | XA1t－02 | $\times 115-02$ |  |  |
| XA14－16 | XA1G－16 | XA1t－03 | Joz－H |  |  |
| XA14－17 | xavor ${ }^{\text {T }}$ | XA 1 C－C4 | XA15－13 |  |  |
| $\times \mathrm{Al4-19}$ | $\times$ AU7－U | xalt－0S | XA14－OS |  |  |
| XA：4－2C | $\times \mathrm{AOB-F}$ | XA $16-\infty$ | XAIE－20 |  |  |
| XA14－21 | XA13－E | XA $1 \in-06$ | xa07－ |  |  |
|  |  | $\times \mathrm{A} 1 \mathrm{t}-07$ |  |  |  |
| A14－23 | XA15－15 | XA $26-08$ | $102-F$ |  |  |
| Als－A | XAJ G－A | －$\times 16-09$ | J02－L |  |  |
| －A1E－A | TEIH－O1 | XA $1 \in-11$ | K A15－16 |  |  |
| XAIE－ e | XA16－6 | xA16－12 | $\times \mathrm{AO} 3-13$ |  |  |
| XA15－${ }^{\text {P }}$ | TEAH－U2 | XA1t－13 | $\times \mathrm{AlS-P}$ |  |  |
| $\times \mathrm{Al}$ ¢ -C | XAOE－C | XA $1 \in-14$ | $\times \mathrm{COS}-\mathrm{E}$ |  |  |
| XA」E－ $\mathbf{D}$ | XAO3－F | XA1E－15 | XA15－m |  |  |
| Yats－E | XA14－ | XA $1 \in-16$ | XA14－16 |  |  |
| A $15-F$ | $\times{ }^{\text {X }}$（4－ 2 | XA1t－17 | $\times \times 15-11$ |  |  |
| $X A 1 E-H$ | xal 6 －J | XA16－18 | $\times$ ¢04－23 |  |  |
| XA1E－H | XAU4－20 | xalt 19 | $\times 145-K$ |  |  |
| XAI $\leq-\checkmark$ | XA16－K | $x$（1te－20 | 」02－N |  |  |

## APPENDIX A

## REFERENCES

| The following publications apply to operation and maintenance of the equipment covered in this manual: DA Pam 310-4 $\qquad$ Index of Technical Manuals, Technical Bulletins, Supply Manuals (types |  |
| :---: | :---: |
|  |  |
| DA Pam 310-7 | U.S. Army Equipment Index of Modification Work Orders |
| NW 00-15PA-1 | Technical Inspection Manual, Soldering for Electric and Electronic Application (Navy) |
| SB 38-100 | Preservation, Packaging and Packing Materials, Supplies, and Equipment Used by the Army |
| TB SIG 222 | Solder and Soldering |
| TB 43-0118 | Field Instructions for Painting and Preserving Electronics Command Equipment |
| TM 38-750 | The Army Maintenance Management System (TAX) |
| TM 11-7440-238-15, | Operator, Organizational, Direct Support, General Support, and Depot |
| TO 31W4-4-1, NAVSHIPS | Maintenance Manual, Digital Subscriber Terminal Sets AN/FYA- |
| 0967-324-0100. | 71(V) 1 through AN/FYA-7 1(V)6 |
| TM 11-7440-239-15, | Operator, Organizational, DS, GS, and Depot Maintenance Manual, |
| TO 31W4-4-11, NAVSHIPS 0967-324-0110. | AUTODIN Digital Subscriber Terminals |
| TO 00-25-234 | General Shop Practice Requirements for the Repair, Maintenance, and Test of Electronic Equipment |
| TB SIG 355-1 | Depot Inspection Standard for Repaired Signal Equipment |
| TB SIG 355-2 | Depot Inspection Standard for Refinishing Repaired Signal Equipment |
| TB SIG 3553 | Depot Inspection Standard for Moisture and Fungus Resistant Treatment |
| TM 740-90-1 | Administrative Storage of Equipment |
| TM 750-244-2 | Procedure for Destruction of Electronic Materiel |

Change 7 A-1/(A2 blank)

## APPENDIX C

## MAINTENANCE ALLOCATION

## Section I. INTRODUCTION

## C-1. General

This appendix provides a summary of the maintenance operations covered in the equipment maintenance manual for Reader, Punched Card RP-152/G. It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

## C-2. Explanation of Format for Maintenance Allocation Chart

a. Group Number. Group numbers correspond to the reference designation prefix assigned in accordance with ASA Y32.16, Electrical and Electronics Reference Designations. They indicate the relation of listed items to the next higher assembly.
b. Component Assembly Nomenclature. This column lists the item names of component units, assemblies, subassemblies, and modules on which maintenance is authorized.
c. Maintenance Function.. This column indicates the maintenance category at which performance of the specific maintenance function is authorized. Authorization to perform a function at, any category also includes authorization to perform that function at higher categories. The codes used represent the various maintenance categories as follows:

## Code

C.
H.........
H.........
D.........
$\qquad$ General support maintenance.
d. Tools and Equipment. The numbers appearing in this column refer to specific tools and equipment which are identified by these numbers in section III.
e. Remarks. Self-explanatory.

## C-3. Explanation of Format for Tool and Test Equipment Requirements

The columns in the tool and test equipment requirements chart are as follows:
a. Tools and Equipment. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool for the maintenance function.
b. Maintenance Category. The codes in this column indicate the maintenance category normally allocated the facility.
c. Nomenclature. This column lists tools, test, and maintenance equipment required to perform the maintenance functions.
d. Federal Stock Number. This column lists the Federal stock number.
e. Tool Number. Not used.

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## SECTION III. TOOL .ND TEST EQUIPMENT REQUIREMENTS



SECTION III. TOOL END TEST EQUIPMENT REQUIREMENTS

| TOOL AND TEST EQUIPMENT REQUIREMENTS |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| TOOLS AND EQUIPMENT | MAINTENANCE CATEGORY | NOMENCLATURE | $\begin{gathered} \text { FEDERAL } \\ \text { STOCK } \\ \text { NUMBER } \end{gathered}$ | TOOL NUMBER |
| 21 | D | RP-152/0 (continued) |  |  |
|  |  | RESISTOR, DECADE (GENERAL RADIO CO. MODEL 1434M) |  |  |
| 2223 | D | EXTENDER, PRINTED CIRCUIT BOARD(GENERAL DYNAMICS/ELECTRONICS N0. 809002-876) |  |  |
|  | D | TEST FACILITY, PRINTED CIRCUIT BOARD |  |  |
|  |  | NOTES: DEPOT MAY SUBSTITUTE EQUIVALENT TEST EQUIPMENT. |  |  |
| AMSEL-MR Form |  | 6013 (Supersedes edition of 1 Jan 65 which is obsolete) |  | ESC-FM 95-66 |
| 1 Jan 66 |  |  |  |  |

## APPENDIX D

## ON-SITE, AREA RESUPPLY, AND DEPOT REPAIR PARTS

## Section I. INTRODUCTION

## D-1. Scope.

a. The equipment covered in this appendix is categorized as a "FIXED STATION INSTALLATION." Maintenance functions have been authorized to site (ORG thru GSU), Area Resupply, and depot.
$\underline{b}$. This equipment is used by electronic service organizations organic to the theater headquarters or communications zones to provide theater communications. Those repair parts authorized up to and including general support maintenance are to be stocked by the organization operating this equipment, therefore a separate display of "Organizational" and "Direct Support" maintenance repair parts would be repetitious and are not included in this appendix.

## D-2. General.

a. The Prescribed Load Allowance (PLA) is not required since this information is adequately defined under "Site Stockage Allowance," Column 7.
b. This list includes all replaceable parts and defines repair parts authorized for maintenance performance at site (ORG and GSU) and depot categories. This list also includes allowances for propositioned resupply of repair parts based on equipment density per geographical locations. This resupply requirement is established to support each Military Department's concentration of DSTE devices to meet the Defense Communication System operational requirement.
c. The repair parts listing is preceded with a cross reference index

## D-3. Explanation of Columns.

An explanation of the columns is given below.
a. Source, Maintenance, and Recoverability Codes (SMR), Column 1. This column lists the applicable SMR codes for the part as follows:

## Change 4 D-1

(1) Source code (A). The source code indicator is the letter appearing on the left in the SMR column. It indicates the source from which the item is obtained in accordance with the following:

## Note:

See para D-3 (4) for cross reference to Air Force SMR codes
Code
Explanation
P- applies to repair parts that are stocked in or supplied from the GSA/DSA, or Army supply system, and authorized for use at indicated maintenance categories.

M - applies to repair parts that are not procured or stocked but are to be manufactured at indicated maintenance categories.

A - applies to assemblies that are not procured or stocked as such but are made up of two or more units, each of which carries an individual stock number and description and is procured and stocked and can be assembled by units at indicated maintenance categories.

X - applies to parts and assemblies that are not procured or stocked; the mortality of which normally is below that of the applicable end item; and the failure of which should result in retirement of the end item from the supply system.

X1 - applies to repair parts that are not procured or stocked, the requirement for which will be supplied by the use of next higher assembly or component.

## Change 4 D-2

## Explanation

X2 - applies to repair parts that are not stocked. The indicated maintenance category requiring such repair parts will attempt to obtain them through cannibalization; if not obtainable through cannibalization; such repair parts will be requisitioned with supporting Justification through normal supply channels.

C - applies to repair parts authorized for local procurement. If not obtainable from local procurement, such repair parts will be requisitioned through normal supply channels with a supporting statement of nonavailability from local procurement.

G - applies to major assemblies that are procured with PEMA funds for initial issue only to be used as exchange assemblies at DSU and GSU category. These assemblies will not be stocked above DSU and GSU category or returned to depot supply category.
(2) Maintenance code (B). The maintenance code indicator is the letter appearing in the center of the SMR column. It indicates the lowest category of maintenance authorized to install the listed item. The codes are:

| Code | Explanation |
| ---: | :--- |
| ${ }^{*}$ C | Operator/Crew |
| *O $^{*}$ F | Organizational Maintenance |
| H | Direct Support Maintenance |
| D | General Support Maintenance |
|  | Depot Support Maintenance |

Note:
*Codes "C" " 0 " and "'F" have not been utilized in this manual. Site maintenance functions have been designated " H " which includes " C " through " F ".
(3) Recoverability code (C). The third, or right hand letter in the SMR column indicates whether the item should be returned for recovery or salvage. Recoverability codes and their explanations are as follows:

## Note:

When no code is indicated in the recoverability column, the part will be considered expendable.

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## Code

## Explanation

R - applies to repair parts and assemblies which are economically repairable at DSU and GSU activities and normally are furnished by supply on an exchange basis.

T - applies to high dollar value recoverable repair parts which are subject to special handling and are issued on an exchange basis. Such repair parts normally are repaired or overhauled at depot maintenance activities.

U - applies to repair parts specifically selected for salvage by reclamation units because of precious metal content, critical materials, high dollar value reusable casings or castings.
(4) Cross reference Army to Air Force SMR code. The following SMR codes represent a cross reference from Army SMR codes displayed in this appendix to appropriate Air Force SMR codes. This coding has been coordinated with OCAMA symbol OCNDTB.


Change 4 D-4
b. Federal Stock Number, Column 2. The Federal stock number for the item is listed in this column.
c.Description, Column 3. This column includes a sequence number, the federal item name, a five-digit Federal supply code for Manufacturer's an indenture code and a part number. The five-digit Federal supply code is followed by the manufacturer's part number. For subsequent appearances of the same item, the manufacturer's code and part number are omitted. The words "same as" followed by the index number assigned to the item when it first appeared in the list will follow the item name, e.g., "RESISTOR, FIXED, COMPOSITION: SAME AS A298." Model column is not used.
d. Unit of Issue, Column 4. The unit used as a basis of issue (e.g., ea, pr, ft, yd, etc.) is indicated in this column.
e. Quantity Incorporated in Unit Pack, Column 5. Not used.
f. Quantity Incorporated in Unit, Column 6. The total quantity of the item used in the equipment is given in this column. Subsequent appearances of the same item in the same assembly are indicated by the letters 'REF".

## NOTE:

1. Effective 30 September 1974, all Federal Stock Numbers listed in the following On-Site, Area Resupply, and Depot Parts List were converted to the 13 -digit National Stock Number (NSN) System.
2. To obtain the 13 -digit NSN by conversion from the 11-digit Federal Stock Number, a National Codification Bureau Code (NCBC) of "GO" will be entered following the Federal Stock Classification (FSC) code (first four digits).
3. An example of coding; and expansion of the FSN to the ,NO is as follows;
a. FSN - 6625-553-0142
b. NCBC - 00
c. FSC -6625
d. NSN - 6625-00-553-0142
4. All replacement parts will be ordered under the NSN System.

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## g. Site Stockage Allowance, Column 7.

(1) The maintenance allowance columns are divided into subcolumns. The total quantity of items authorized for the number of equipments supported is indicated in each subcolumn opposite the first appearance of each item. Subsequent appearances of the same item will have no entry in the allowance columns, but will have a reference in the description column to the first appearance of the item. Items authorized for use as required, but not for initial stockage, are identified with an asterisk (*) in the allowance column.
(2) The quantitative allowances for Site (ORG thru GSU) maintenance represents one initial prescribed load for the number of equipments supported.
(3) Subsequent changes to Site (ORG thru GSU), allowances will be limited as follows: No change in the range of items is authorized. If additional items are considered necessary, recommendation should be forwarded to Commanding General, U. S. Army Electronics Command, ATTN: AMSEL-ME-NMP-CW, Fort Monmouth, N. J. 07703, for exception or revision to the allowance list. Revisions to the range of items authorized will be made by USAECOM National Maintenance Point based upon engineering experience, demand data, or TAERS information.
h. Forty-five Day Area Resupply Allowance Based on Number of DSTE Devices Supported, Column 8.
(1) The allowance column is divided into three subcolumns. The total quantity of items authorized for the number of equipments supported is indicated in each subcolumn opposite the first appearance of each item.
(2) The quantitative resupply allowances for the area resupply, represents one initial prescribed load for the number of DSTE equipments to be supported.

## D-6 Change 4

(3) Subsequent changes to Area Resupply allowances will be limited as follows: No change in the range of items is authorized. If additional items are considered necessary, recommendation should be forwarded to Commander, US Army Electronics Command, ATTN: AMEL-MA-CW, Fort Monmouth, New Jersey 07703, for exception or revision to the allowance list. Revisions to the range of items authorized will be made by USAECOM National Maintenance Point based upon engineering experience, demand data, or TAERS information.
i. One-Year Allowances Per 100 Equipments/Contingency Planning Purposes, Column 9. Contingency planning requirements must be computed on a per equipment basis for fixed plant equipment, therefore column 9 will be utilized. Contingency Plan requirements for this equipment will be satisfied by furnishing one load of repair parts per quantities displayed under column 7, Site Stockage Allowance.
j. Depot Maintenance Allowance Per 100 Equipments, Column 10. This column indicates the total quantity of each item authorized depot maintenance for 100 equipments. Subsequent appearances of the same item will have no entry in this column, but will have a reference in the description column to the first appearance of the item.
k. Illustrations. Column 11.
(1) Figure number column 11a. The number of the illustration in which the item is shown is indicated in this column.
(2) Item No. or reference designation, column 11b, The callout number or reference designation used to reference the item in the illustration appears in this column.

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## SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER

| FIG. NO. | $\qquad$ | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ | FIG. NO. | $\begin{gathered} \text { ITEM NO. } \\ \text { OR } \\ \text { REFERENCE } \\ \text { DESIGNATION } \\ \hline \end{gathered}$ | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4-1 | 1 | A757 |  | 44 | A815M |
|  |  | A829 |  | 45 | A748 |
|  | 3 | A828 |  | 46 | C023 |
|  | 4 | A827 |  | 47 | C041 |
|  | 5 | A830 |  | 48 | A749 |
|  | 6 | B260A |  | 49 | A751A |
|  | 7 | A832 |  | 50 | A750 |
|  | 8 | A835 |  | 51 | A752 |
|  | 9 | A833 |  | 52 | A753 |
|  | 10 | A834M |  | 53 | A753B |
|  | 11 | B256 |  | 54 | A753D |
|  | 11.1 | A831A |  | 55 | A753E |
|  | 12 | A826 |  | 56 | A753F |
|  | 13 | A002C |  | 57 | A753G |
|  | 14 | A002D |  | 58 | A753C |
|  | 14.1 | A002B |  | 59 | A754 |
|  | 15 | A002A |  | 60 | A755 |
|  | 16 | A686 |  | 61 | A755D |
|  | 17 | A687 |  | 62 | A756 |
|  | 18 | A688 |  | 63 | A821B |
|  | 19 | A685 |  | 64 | B970 |
|  | 20 | B261A |  | 64.1 | B970A |
|  | 21 | B966 |  | 65 | B972 |
|  | 22 | B968M |  | 66 | B973 |
|  | 23 | B967 |  | 67 | B974 |
|  | 24 | B965D |  | 68 | B975 |
|  | 24.1 | B965F |  | 69 | B976 |
|  | 24.2 | B965C |  | 70 | B977 |
|  | 24.3 | B965E |  | 71 | B978 |
|  | 24.4 | B965B |  | 72 | B971 |
|  | 24.5 | B965G |  | 73 | B979 |
|  | 28 | A792 |  | 73.1 | B989 |
|  | 29 | A789M |  | 73.2 | B991 |
|  | 30 | A764C |  | 74 | B992 |
|  | 31 | A764B |  | 75 | B994 |
|  | 31.1 | A764A |  | 76 | B987 |
|  | 32 | A764M |  | 77 | B997 |
|  | 33 | A762 |  | 78 | B999A |
|  | 34 | A758A |  | 79 | B998 |
|  | 34.1 | A759 |  | 80 | B995 |
|  | 34.2 | A760 |  | 81 | B996 |
|  | 34.3 | A761A |  | 82 | C003 |
|  | 35 | B962 |  | 83 | C004A |
|  | 36 | B963 |  | 84 | C005A |
|  | 37 | B964 |  | 85 | C001A |
|  | 38 | B961 |  | 86 | C009 |
|  | 38.1 | B961A |  | 87 | C008 |
|  | 38.2 | B961B |  | 88 | C010A |
|  | 38.3 | B961C |  | 89 | C011 |
|  | 38.4 | B961D |  | 90 | C010 |
|  | 38.5 | B961E |  | 91 | C014 |
|  | 39 | B969 |  | 92 | C015 |
|  | 40 | A747A |  | 93 | C016 |
|  | 41 | A812A |  | 94 | C017 |
|  | 42 | C021 |  | 95 | C012 |
|  | 43 | C039 |  | 96 | C013M |

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SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE
TO INDEX NUMBER (CONTINUED)
ITEM NO.
OR


FIG.
NO.
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| $\begin{gathered} \text { ITEM NO. } \\ \text { OR } \\ \text { REFERENCE } \\ \text { DESIGNATION } \\ \hline \end{gathered}$ | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ |
| :---: | :---: |
| 97 | C018 |
| 98 | C020 |
| 99 | C019 |
| 100 | C022 |
| 101 | C030 |
| 102 | C036 |
| 103 | C040 |
| 104 | C048 |
| 105 | C054 |
| 106 | C055 |
| 107 | C056 |
| 108 | C057 |
| 109 | C058 |
| 110 | C062 |
| 111 | C063 |
| 112 | C064 |
| 113 | C061 |
| 114 | C066 |
| 115 | C067 |
| 116 | C068 |
| 117 | C069 |
| 118 | C112 |
| 119 | C065 |
| 120 | C070 |
| 121 | C074 |
| 122 | C083 |
| 123 | C092 |
| 124 | C096 |
| 125 | C100 |
| 126 | C108 |
| 1 | A520 |
| 2 | A632 |
| 3 | A565 |
| 3.1 | A631A |
| 4 | A357 |
| 4.1 | A519A |
| 5 | A024 |
| 6 | A235 |
| 7 | A163 |
| 8 | A127 A097 |
| ${ }_{10}^{9}$ | A097 A003 |
| 11 | A257A |
| 12 | A291 |
| 13 | A189 |
| 14 | A651 |
| 15 | A682 |
| 15.1 | A682A |
| 16 | A683A |
| 17 | A648 ${ }_{\text {A649M }}$ |
| 19 | A650 |
| 20 | A647 |
| 20.1 | A681 |
| 20.2 | A680A |

FIG.
NO.
4-2



ITEM NO.


INDEX
NO.
A667A
A678
A677
A679
A679A
A676B
A675
A669
A670
A671
A672B
A668B
A674
A653A
A653DM
A653B
A653C
A653E
A653F
A656A
A656B
A656
A659
A660
A661
A658
A657
A652A
A657A
A657B
A657C
A657D
A657E
A657F
A657G
A657H
A646A
A646B
A646C
A653G
A646
A666
A642A
A662A
A651A
A652
A744M
A736M
A728M
A716M
A732M
A720M
A724M
A740M
A703M

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SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER (CONTINUED)

| FIG. $\frac{\mathrm{NO}}{4-3}$ | $\begin{gathered} \text { ITEM NO. } \\ \text { OR } \\ \text { REFENCE } \\ \frac{\text { DESIGNATION }}{10} \end{gathered}$ | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ | FIG. NO. | $\begin{gathered} \text { ITEM NO. } \\ \text { OR } \\ \text { REFENCE } \\ \frac{\text { DESIGNATION }}{40} \end{gathered}$ | $\begin{aligned} & \text { INDEX } \\ & \frac{\text { NO. }}{\text { B611 }} \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | 11 | A698M |  | 40 41 | B265A |
|  | 12 | A702 M |  | 42 | B271A |
|  | 13 | A704M |  | 43 | B267M |
|  | 14 | A690M |  | 44 | B266 |
|  | 15 | A694M |  | 45 | B264A |
|  | 16 | A708M |  | 45.1 | B279A |
|  | 17 | A745M |  | 46 | B268 |
|  | 18 | A689 |  | 47 | B274 |
|  | 19 | A745A |  | 48 | B263 |
|  | 20 | A756B |  | 49 | B262 |
|  | 21 | A756C |  | SO | B286A |
|  | 22 | A756D |  | 51 | B287B |
|  | 23 | A756A |  | 52 | B287C |
|  | 24 | A755A |  | 53 | B285A |
|  | 25 | A755B |  | 54 | B287A |
|  | 26 | A755C |  | 55 | B280 |
| 4-4 | 1 | B841E |  | 56 57 | B281 B 283 |
|  | 2 | B841G |  | 58 | B284A |
|  | 3 | B841F |  | 59 | B445 |
|  | 4 | B841D |  | 60 | B447 |
|  | 4.1 | B842A |  | 61 | B446 |
|  | 5 | B875 |  | 62 | B444A |
|  | 5.1 | B875A |  | 62.1 | B448A |
|  | 6 | B861 |  | 62.2 | B449 |
|  | 7 | B867 |  | 62.3 | B451 |
|  | 8 | G862 |  | 62.4 | B450 |
|  | 9 | B868A |  | 62.5 | B456A |
|  | 10 | B871A |  | 62.6 | B457A |
|  | 11 | B854B |  | 62.7 | B458 |
|  | 12 | B857B |  | 62.8 | B460 |
|  | 13 | B848A |  | 62.9 | B459 |
|  | 14 | B850A |  | 62.10 | B8511 |
|  | 15 | B903 |  | 62.11 | B584A |
|  | 16 | B905M |  | 63 | B911A |
|  | 17 | B904 |  | 64 | B913 |
|  | 18 | B902 |  | 65 | B912 |
|  | 19 | B844A |  | 66 | B910A |
|  | 20 | B843A |  | 67 | B907 |
|  | 21 | B898M |  | 68 | B909 |
|  | 22 | B900 |  | 69 | B908 |
|  | 23 | B899 |  | 70 | B906A |
|  | 24 | B897A |  | 71 | B901 |
|  | 25 | B915C |  | 72 | B943M |
|  | 26 | B914A |  | 73 | B945 |
|  | 27 | B918A |  | 74 | B944 |
|  | 28 | B923A |  | 75 | B942A |
|  | 29 | B925 |  | 76 | B946B |
|  | 30 | B924 |  | 77 | B935 |
|  | 31 | B928B |  | 78 | B937E |
|  | 32 | B9228 |  | 78.1 | B937C |
|  | 33 | B927M |  | 78.2 | B937B |
|  | 34 | B894 |  | 78.3 | B937A |
|  | 35 | B896 |  | 78.4 | B941B |
|  | 36 | B895 |  | 78.5 | B941A |
|  | 37 | B893 |  | 79 | B937 |
|  | 38 | B892 |  | 80 | B936 |
|  | 39 | ${ }^{\text {B89 }}$ |  |  |  |


|  | SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER (CONTINUED) |  |  |  |  |
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|  | ITEM NO. |  |  | ITEM NO. |  |
| FIG. NO. | REFERENCE DESIGNATION | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ | FIG. NO. | REFERENCE DESIGNATION | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ |
| 4-4 | 81 | B934 | 4-5 | 22 | A823M |
|  | 82 | B938A |  |  |  |
|  | 83 | B816 | 4-6 | 1 | A786A |
|  | 83.1 | B817M |  | 2 | A786B |
|  | 83.2 | B819 |  | 3 | A786C |
|  | 83.3 | B818 |  | 4 | A787M |
|  | 84 | B815 |  | 4.1 | A788M |
|  | 84.1 | B793A |  | 5 | A769 |
|  | 85 | B794 |  | 6 | A767 |
|  | 86 | B796 |  | 7 | A772 |
|  | 87 | B795 |  | 8 | A775 |
|  | 88 | B7938 |  | 9 | A774 |
|  | 89 | B878 |  | 10 | A773 |
|  | 90 | B880 |  | 11 | A771B |
|  | 91 | B879 |  | 12 | A776 |
|  | 92 | B295B |  | 13 | A778 |
|  | 93 | B333B |  | 14 | A781 |
|  | 94 | B402B |  | 15 | A780 |
|  | 95 | B876 |  | 16 | A779 |
|  | 96 | B877 |  | 17 | A777B |
|  | 97 | B955A |  | 18 | A782 |
|  | 98 | B955C |  | 19 | A766 |
|  | 99 | B9558 |  |  |  |
|  | 100 | B953 | 4-7 |  | B236 |
|  | 101 | B955 |  | 2 | B236 |
|  | 102 | B954A |  | 3 | B235B |
|  | 103 | B952A |  | 4 | B235D |
|  | 104 | B289B |  | 5 | B235C |
|  | 105 | B290 |  | 6 | B235A |
|  | 106 | B291 |  | 7 | B226A |
|  | 107 | B292 |  | 8 | B214 |
|  | 108 | B293 |  | 9 | B149W5 |
|  | 109 | B294 |  | 10 | B149W4 |
|  | 110 | B288B |  | 11 | B149W3 B149W1 |
|  | 1 | A806 |  | 12.1 | B149W2 |
|  | 2 | A809 |  | 12.2 | B149W |
|  | 3 | A807 |  | 13 | B149V |
|  | 4 | A808 |  | 13.1 | B236 |
|  | 5 | A811A |  | 14 | B149V |
|  | 6 | A805B |  | 14.1 | B236 |
|  | 7 | A810A |  | 15 | B228A |
|  | 8 | A794 |  | 15.1 | B149W6 |
|  | 9 | A796 |  | 16 | B231 |
|  | 10 | A795 |  | 17 | B235 |
|  | 11 | A798 |  | 18 | B234 |
|  | 12 | A803 |  | 19 | B232 |
|  | 13 | A793B |  | 20 | B233 |
|  | 14 | A797A |  | 21 | B230A |
|  | 15 | A812 |  | 21.1 | B182 |
|  | 16 | A811C |  | 21.2 | B183 |
|  | 17 | A811E |  | 22 | B181 |
|  | 18 | A811D |  | 23 | B180A |
|  | 19 | A811B |  | 23.1 | B198A |
|  | 20 | A813M |  | 24 | B153 |
|  | 21 | A814M |  | 25 | B155 |

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| FIG. NO. | $\begin{gathered} \text { ITEM NO. } \\ \text { OR } \\ \text { REFERENCE } \\ \text { DESIGNATION } \\ \hline \end{gathered}$ | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ | FIG. NO. |  | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4-7 | 26 | B154 | 4-7 | 74 | B113 |
|  | 27 | B157 |  | 75 | B112 |
|  | 28 | B160 |  | 76 | B120 |
|  | 29 | B159 |  | 77 | B116 |
|  | 30 | B158A |  | 78 | B115 |
|  | 31 | B156 |  | 79 | B111 |
|  | 32 | B161 |  | 80 | B119 |
|  | 33 | B163 |  | 81 | B111 |
|  | 33.1 | B152 |  | 82 | B121 |
|  | 34 | B124 |  | 82.1 | B107 |
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|  | 36 | B125 |  | 84 | B076 |
|  | 37 | B122A |  | 85 | B075 |
|  | 38 | B236 |  | 86 | B250A |
|  | 39 | B236 |  | 87 | B250A |
|  | 39.1 | B163A |  | 88 | B082 |
|  | 40 | B225A |  | 89 | B092 |
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|  | 42 | B148T |  | 91 | B089 |
|  | 43 | B148FM |  | 92 | B088 |
|  | 44 | B146 |  | 93 | B084 |
|  | 45 | B148 |  | 94 | B086 |
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|  | 47 | B145B |  | 96 | B090A |
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|  | 59 | B133 |  | 108 | B094A |
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|  | 60 | B141 |  | 110 | B088 |
|  | 61 | B143 |  | 111 | B087 |
|  | 61.1 | B142 |  | 112 | B097 |
|  | 62 | B139 |  | 113 | B093 |
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|  | 63.1 | B141A |  | 114.1 | B081 |
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|  | 64 | B144 |  | 116 | B083A |
|  | 64.1 | B123B |  | 117 | B077A |
|  | 64.2 | B127 |  | 118 | B078 |
|  | 65 | B206AM |  | 119 | B079 |
|  | 66 | B205AM |  | 119.1 | B073A |
|  | 67 | B108 |  | 120 | A914 |
|  | 68 | B110 |  | 121 | A916 |
|  | 69 | B109 |  | 122 | A915 |
|  | 70 | B117 |  | 123 | A918A |
|  | 71 | B117 |  | 124 | A920 |
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|  |  | Chan |  |  |  |

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## SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER (CONTINUED)

| $\begin{aligned} & \text { FIG. } \\ & \text { NO. } \end{aligned}$ |  | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ | FIG. NO. |  | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ |
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| 4-7 | 235 | B208 | 4-8 | 1 | B148X |
|  | 236 | B209 |  | 2 | B1481 |
|  | 237 | B207 |  | 3 | B1484 |
|  | 238 | B242 |  | 4 | B184 |
|  | 239 | B239 |  | 5 | B148W |
|  | 240 | B241 |  | 6 | B148V |
|  | 241 | B240 |  | 7 | B1485 |
|  | 242 | B238 |  | 8 | B1486 |
|  | 243 | B237 |  | 9 | B148Y |
|  | 244 | A909 |  |  |  |
|  | 245 | A910 | 4-10 | 1 | B149T |
|  | 246 | A908 |  | 1.1 | B149S |
|  | 246.1 | A911B |  | 2 | B149RM |
|  | 246.2 | A912 |  | 3 | B149QM |
|  | 247 | A907 |  | 4 | B149M |
|  | 248 | B195 |  | 5 | B149PM |
|  | 249 | B197 |  | 6 | B149L |
|  | 250 | B196 |  | 7 | B149KM |
|  | 251 | B192 |  | 8 | B149N |
|  | 251. | B199A |  | 8.1 | B149H |
|  | 252 | B1164 |  | 9 | B149GM |
|  | 255 | B244 |  | 10 | B149JM |
|  | 256 | B246 |  | 11 | B149FM |
|  | 257 | B245 |  | 13 | B149DM |
|  | 258 | B243 |  | 14 | B151 |
|  | 259 | B211 |  | 15 | B150 |
|  | 260 | B213 |  | 16 | B148EA |
|  | 261 | B212 |  | 17 | B148EB |
|  | 262 | B210 |  | 18 | B14BEF |
|  | 263 | B216 |  | 19 | B14BED |
|  | 264 | B218 |  | 19.1 | B148EG |
|  | 265 | B217 |  | 20 | B148EE |
|  | 2G6 | B215 |  | 21 | B148EC |
|  | 267 | B21] |  | 22 | B148BM |
|  | 268 | A924 |  | 23 | B148A |
|  | 269 | A926 |  | 24 | B148DM |
|  | 270 | A925 |  | 25 | B149B |
|  | 270.1 | A933 | 4-11 | 1 | B072 |
|  | 270.2 | A928 |  | 2 | B071 |
|  | 271 | A929 |  | 3 | A940 |
|  | 271.1 | A927 |  | 3.1 | B072B |
|  | 272 | A923 |  | 4 | A960 |
|  | 273 | B163C |  | 5 | A962 |
|  | 274 | B163E |  | G | A961 |
|  | 275 | B163D |  | 7 | A963 |
|  | 276 | B163B |  | 8 | A964 |
|  | 277 | B186 |  | 9 | A959 |
|  | 278 | B187 |  | 9.1 | A965 |
|  | 279 | B185A |  | 10 | A968 |
|  | 280 | B224 |  | 11 | A968 |
|  | 281 | B224 |  | 12 | A967 |
|  | 282 | B251 |  | 13 | P969 |
|  |  |  |  | 14 | A956 |

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| FIG. NO. |  | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ | FIG. <br> NO. |  | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4-11 | 14.1 | A957 |  | 51 | B033 |
|  | 14.2 | A958 |  | 51.1 | B034 |
|  | 15 | A955 |  | 52 | B032A |
|  | 16 | A970 |  | 53 | B039AM |
|  | 17 | A954A |  | 54 | B057A |
|  | 18 | A953 |  | 55 | B056 |
|  | 18.1 | A951 |  |  |  |
|  | 18.2 | A950 |  | 56 | B038AM |
|  | 19 | A952 | 4-11 | 57 | B053 |
|  | 20 | A947 |  | 58 | B052 |
|  | 20.1 | A948 |  | 59 | B036A |
|  | 20.2 | A949A |  | 60 | B059 |
|  | 21 | A946 |  | 61 | B058 |
|  | 22 | A971 |  | 62 | B062A |
|  | 23 | A945A |  | 63 | B051A |
|  | 24 | A944 |  | 64 | B066 |
|  | 24.1 | A942 |  | 64.1 | B072A |
|  | 24.2 | A941 |  | 65 | B035 |
|  | 25 | A943A |  | 66 | B040 |
|  | 26 | A972A |  | 67 | B060A |
|  | 26.1 | A939 |  | 68 | B063 |
|  | 27 | B042 |  | 69 | B048 |
|  | 28 | B043 |  | 70 | B050 |
|  | 29 | B049 |  | 71 | B049 |
|  | 30 | B068 |  | 72 | B047 |
|  | 31 | B070 |  | 73 | B065 |
|  | 32 | B069 |  | 74 | B064 |
|  | 33 | B067 |  | 75 | B046 |
|  | 34 | B021 |  | 76 | B061 |
|  | 34A | B024 |  | 77 | B072F |
|  | 34B | B023 |  | 78 | B072C |
|  | 35 | B020 |  | 79 | B072D |
|  | 36 | B022 |  | 80 | B045A |
|  | 37 | A979 | 5-2 | A13 | A003 |
|  | 38 | A978 | 5-3 | A6 | A024 |
|  | 38.1 | A977M | 5-4 | A8 | A163 |
|  | 39 | B026 | 5-5 | A10 | A097 |
|  | 40 | A974 |  | A12 | A112 |
|  | 41 | A976 | 5-6 | A9 | A127 |
|  | 42 | A975 |  | A11 | A145 |
|  | 43 | B025 | 5-7 | A16 | A189 |
|  | 44 | B027 | 5-8 | A7 | A235 |
|  | 44.1 | A973M | 5-9 | A14 | A257A |
|  | 45 | B044 | 5-10 | A15 | A291 |
|  | 46 | B029 | 5-11 | A5 | A357 |
|  | 47 | B028M | 5-12 | A1 | A520 |
|  | 47.1 | B028N | 5-13 | A4 | A565 |
|  |  | B055 | 5-13.1 | A4 | A631A |
|  | 49 | B054 | 5-13.2 | A5 | A519A |
|  | 50 | B037 |  |  |  |

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| FIG. NO. | $\begin{gathered} \text { ITEM NO. } \\ \text { OR } \\ \text { REFERENCE } \\ \text { DESIGNATION } \end{gathered}$ | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ | FIG. NO. | $\begin{gathered} \text { ITEM NO. } \\ \text { OR } \\ \text { REFERENCE } \\ \text { DESIGNATION } \\ \hline \end{gathered}$ | INDEX NO. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 5-14 | A3 | A632 | 5-19 | C 2 C 3 | B520M B521M |
| 5-15 | PS1A1 | B295B |  | C4 | B522M |
| 5-16 | PS1A2 | B333B |  | CR1 CR2 | B533 B534 |
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| 5-17 | PS1A3 | B402B |  | CR4 | B536 |
|  | PS1A4 | B457A |  | E1 E2 | B559 B560 |
| 5-18 | C1 | B465M |  |  |  |
|  | C2 | B466M |  |  |  |
|  | C3 | B468M |  | ES | B563 |
|  | C4 | B467A |  | E6 | B583 |
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|  | CR3 | B479M |  | E9 | B566 |
|  | CR4 | B478 |  | E10 | B567 |
|  | E1 | B494 |  | E11 | B568 |
|  | E2 | B495 |  | E12 | B569 |
|  | E3 | B496 |  | E13 | B570 |
|  | E4 | B510 |  | E14 | B571 |
|  | E5 | B497 |  | E15 | B572 |
|  | E6 | B498 |  | E16 | B573 |
|  | E7 | B499 |  | E17 | B574 |
|  | E8 | B500 |  | E18 | B575 |
|  | E9 | B501 |  | E19 | B576 |
|  | E10 | B502 |  | E20 | B577 |
|  | E11 | B503 |  | E21 | B578 |
|  | E12 | B504 |  | E22 | B579 |
|  | E13 | B505 |  | E23 | B580 |
|  | E14 | B506 |  | E24 | B581 |
|  | E15 | B507 |  | E25 | B582 |
|  | E16 | B508 |  | H1 | B515A |
|  | E17 | B509 |  | H2 | B516 |
|  | H1 | B461A |  | H3 | B517 |
|  | H2 | B462 |  | H4 | B518 |
|  | H3 | B463 |  | H5 | B525A |
|  | H4 | B464 |  | H6 | B526 |
|  | H5 | B471A |  | H7 | B541 |
|  | H6 | B491A |  | H8 | B548A |
|  | H7 | B491B |  | H9 | B556D |
|  | H8 | B492 |  | H10 | B556E |
|  | H9 | B493A |  | H11 | B556F |
|  | H10 | B510A |  | H12 | B557A |
|  | P1 | B469 |  | H13 | B558A |
|  | P2 | B470 |  | H14 | B583A |
|  | Q1 | B480 |  | P1 | B523 |
|  | Q2 | B484 |  | P2 | B524 |
|  | Q3 | B488 |  | Q1 | B537 |
|  | R1 | B472B |  | Q2 | B542 |
|  | R2 | B473B |  | Q3 | B547 |
|  | R3 | B474M |  | Q4 | B552 |
|  | R4 | B475C |  | R1 | B527A |
|  | PS1A5 | B511 |  | R2 | B532A |
|  |  |  |  | R3 | B529 B532B |
| 5-19 | C1 | B519M |  | R4 | B532B |

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| FIG. NO. |  | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ | FIG. NO. | $\begin{gathered} \text { ITEM NO. } \\ \text { OR } \\ \text { REFERENCE } \\ \text { DESIGNATION } \\ \hline \end{gathered}$ | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 5-19 | $\begin{aligned} & \text { R5 } \\ & \text { R6 } \\ & \text { R7 } \end{aligned}$ | $\begin{aligned} & \text { B528A } \\ & \text { B532M } \\ & \text { B531M } \end{aligned}$ | 5-22A | $\begin{aligned} & \text { R1 } \\ & \text { R2 } \\ & \text { R3 } \end{aligned}$ | $\begin{aligned} & \text { B804D } \\ & \text { B808A } \\ & \text { B809A } \end{aligned}$ |
| 5-20 | PS1A6 <br> E1 <br> E3 <br> E4 <br> E5 <br> E6 <br> E8 <br> H1 <br> H2 <br> H3 <br> H4 <br> $H 5$ $H 6$ <br> H6 H7 <br> P1 <br> Q1 <br> Q2 <br> R1 <br> R2 | B584A <br> B604 <br> B605 <br> B606 <br> B607 <br> B608 <br> B609 <br> B610 <br> B610A <br> B588A <br> B589 <br> B590 <br> B593A <br> B602 <br> B603 <br> B592 <br> B597 <br> B601 <br> B595B <br> B596A | 5-22B | A15 C1 C2 C4 C5 CR1 CR2 CR3 CR4 R1 R2 R3 R4 R5 R6 R7 R9 R10 R11 R12 | B820A B821 B822 B823 B824 B825 B837 B838 B839 B840 B826 B827A B828AA B829A B835M B83AA B834A B833B B832M B832A B836A B833A |
| 5-21 | PS1A12 | B611A |  |  |  |
| 5-22A | A14 <br> CR1 <br> CR2 <br> CR3 <br> CR4 <br> E1 <br> E2 <br> E4 <br> H1 <br> H2 <br> H3 <br> H4 <br> H5 <br> H6 <br> H7 <br> H8 <br> H9 <br> H10 <br> H11 <br> H12 <br> J5 <br> J6 <br> J7 <br> J8 | B797A <br> B810M <br> B812M <br> B813M <br> B798 <br> B799 <br> B801 <br> B802 <br> B803C <br> B805A <br> B806 <br> B807 <br> B807A <br> B814M <br> B814A <br> B814B <br> B815F <br> B815A <br> B815B <br> B815D <br> Change | 8 blank) |  |  |



TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-21



035

TM 11-7440-215-15/NAVSHIPS 0967-324-0@23/TO 31W4-2G-21


CB


| TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-21 |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |

(11)

| (5) |  |
| :---: | :---: |
|  |  |
|  |  |
|  |  |
|  | QTY |
| S | INC |
| U | INIT |
| UNI |  |
| PK |  |

(6)
(8) (30 DAYS)
SITE STOCKAGE

ALLOWANCE | $\begin{array}{c}\text { 45 DAY AREA }\end{array}$ |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :---: | :---: | :---: |
| RESUPPLY ALLOW |  |  |  |  |  |  |
| BASED ON NO. |  |  |  |  |  |  |
| EQUIP. SUPPORTED |  |  |  |  |  |  | (9)

1 YEAR
ALW
PER 100
EQUIP
CNTGC
PLAN
(10)
EA

- RE

|  | $1-5$ | $6-10$ | $11-2$ |
| :--- | :--- | :--- | :--- |
|  |  |  |  |
|  |  |  |  |

$\rightarrow$
EA

REF
EA

EA
REF

EA
EA RE


|  | EQ |
| :--- | :--- |
|  |  |


| -15 |
| :---: |
| $5-3$ |
| -15 |
| $5-3$ |
|  |
|  |
|  |
|  |

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|  |  |  | REPAIRS PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  | (4)U$N$1$T$OF1$S$$S$$S$$U$$E$ | (5) |  | (7)SITE0 DAYS)ALLOCKAGEALLOWANCE |  |  | (8) <br> 45 DAY AREA RESUPPLY ALLOW BASED ON NO. EQUIP. SUPPORTED |  |  | (9) <br> 1 YEAR ALW EQUIP CNTGCY | (10) <br> DEPOT MAINT ALW PER 100 EQUIP | (11) <br> ILLUSTRATION |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | MODEL |  |  | $\begin{array}{\|c} \mathbf{N} \\ \mathbf{D} \\ \mathbf{C} \\ \mathrm{D} \end{array}$ | DESCRIPTION |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  | 234 |  |  |  |  | (A) |  |  |  |  |  | (B) |  |  |  |  |
|  |  |  | STOCK |  |  |  |  |  |  | (A) |  |  | (B) | $\underset{11-20}{(C)}$ | (A) |  |  |  | ${ }_{6-10}^{(B)}$ |  | ${ }_{11-20}^{(C)}$ | FIG. | ORREF |
| P | D |  | 59057235251 |  |  |  | D | A051 | RESISTOR, FIXED, COMPOSITION: <br> 81349; RC07GF222J |  | EA |  | 24 |  |  |  |  |  |  |  |  | 66 | -15 | R2 |
|  |  |  | 59057235251 |  |  |  | D | A052 | RESISTOR, FIXED, COMPOSITION: SAME AS A051 |  | EA |  | REF |  |  |  |  |  | - |  |  | $\begin{array}{r}15 \\ \hline 5-3\end{array}$ | R4 |
|  |  |  | 59057235251 |  |  |  | D | A053 | RESISTOR, FIXED, COMPOSITION: SAME AS A051 | EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $5-3$ | R6 |
|  |  |  | 59057235251 |  |  |  | D | A054 | RESISTOR, FIXED, COMPPSITION: SAME AS A051 | EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $5-3$ | R8 |
|  |  |  | 59057235251 |  |  |  | D | A055 | RESISTOR, FIXED, COMPOSITION: SAME AS A051 | EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $5-3$ | R10 |
|  |  |  | 59057235251 |  |  |  | D | A056 | RESISTOR, FIXED, COMPOSITION: SAME AS A051 | EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $5-3$ | R12 |
|  |  |  | 59057235251 |  |  |  | D | A057 | RESISTOR, FIXED, COMPOSITION: SAME AS A051 | EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> -3 | R14 |
|  |  |  | 59057235251 |  |  |  | D | A058 | RESISTOR, FIXED, COMPOSITION: SAME AS A051 | EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $5-3$ | R16 |
|  |  |  | 59057235251 |  |  |  | D | A059 | RESISTOR, FIXED, COMPOSITION: SAME AS A051 | EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> -3 | R18 |
|  |  |  | 59057235251 |  |  |  | D | A060 | RESISTOR, FIXED, COMPOSITION: SAME AS A051 | EA |  | REF |  |  |  |  |  |  |  |  | 5-3 | R20 |



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\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{\multirow[t]{4}{*}{}} \& \multicolumn{7}{|r|}{REPAIRS PARTS FOR ON-SITE, AREA RESUPPLY,
AND DEPOT MAINTÉNANCE} \& \multirow[t]{4}{*}{} \& \multirow[t]{4}{*}{\[
\begin{gathered}
\text { (5) } \\
\\
\\
\text { QTY } \\
\text { INC } \\
\text { IN } \\
\text { UNIT } \\
\text { PK }
\end{gathered}
\]} \& \multirow[t]{4}{*}{\begin{tabular}{l}
(6) \\
QTY INC IN
\end{tabular}} \& \multicolumn{3}{|l|}{\multirow[t]{3}{*}{\begin{tabular}{l}
(7) \\
(30 DAYS) SITE STOCKAGE ALLOWANCE
\end{tabular}}} \& \multicolumn{3}{|l|}{\multirow[t]{3}{*}{\begin{tabular}{|c|} 
(8) \\
45 DAY AREA \\
RESUPLY ALLOW \\
BASED ONNO. \\
EQUIP. SUPPORTED
\end{tabular}}} \& \multirow[t]{4}{*}{(9)

1 YEAR
ALW
PER 100
EQUIP
CNTGCY

PLAN} \& \multirow[t]{4}{*}{} \& \multicolumn{2}{|l|}{\multirow[t]{2}{*}{| (11) |
| :---: |
| ILLUSTRATION |}} <br>

\hline \& \& \& \multirow[t]{3}{*}{| (2) |
| :--- |
| FEDERAL STOCK NUMBER |} \& \multicolumn{3}{|r|}{MODEL} \& \& \& (3) \& \& \& \& \& \& \& \& \& \& \& \& \& <br>

\hline \& \& \& \& \& \& \& N \& \& \& \& \& \& \& \& \& \& \& \& \& \& (A) \& (B) ${ }_{\text {ITEM }}$ <br>

\hline \& \& \& \& 12 \& \& 56 \& C \& \& DESCRIPTION \& \& \& \& $$
\begin{gathered}
\text { (A) } \\
1-5
\end{gathered}
$$ \& \[

$$
\begin{array}{|c|c|}
(\mathrm{B}) \\
6-10
\end{array}
$$

\] \& \[

\underset{11-20}{(C)}

\] \& \[

$$
\begin{gathered}
\text { (A) } \\
1-5
\end{gathered}
$$

\] \& \[

\left\lvert\, $$
\begin{gathered}
\text { (B) } \\
6-10
\end{gathered}
$$\right.

\] \& \[

$$
\begin{gathered}
\text { (C) } \\
11-20
\end{gathered}
$$
\] \& \& \& FIG.

No. \& OR REF <br>

\hline \& \& \& 59618140768 \& \& \& \& D \& A071 \& SEMI-CONDUCTOR DEVICE, DIODE: SAME AS A066 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| :---: |
| -3 | \& CR6 <br>


\hline \& \& \& 59618140768 \& \& \& \& D \& A072 \& SEMI-CONDUCTOR DEVICE, DIODE: SAME AS A066 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| -3 | \& CR7 <br>


\hline \& \& \& 59618140768 \& \& \& \& D \& A073 \& SEMI-CONDUCTOR DEVICE, DIODE: SAME AS A066 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-3$ | \& CR8 <br>


\hline \& \& \& 59618140768 \& \& \& \& D \& A074 \& SEMI-CONDUCTOR DEVICE, DIODE: SAME AS A066 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| -3 | \& CR9 <br>


\hline \& \& \& 59618140768 \& \& \& \& D \& A075 \& SEMI-CONDUCTOR DEVICE, DIODE: SAME AS A066 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-3$ | \& CR10 <br>


\hline \& \& \& 59618140768 \& \& \& \& D \& A076 \& SEMI-CONDUCTOR DEVICE, DIODE: SAME AS A066 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| -3 | \& CR11 <br>


\hline \& \& \& 59618140768 \& \& \& \& D \& A077 \& SEMI-CONDUCTOR DEVICE, DIODE: SAME AS A066 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| :---: |
| $5-3$ | \& CR12 <br>


\hline \& \& \& 59618140768 \& \& \& \& D \& A078 \& SEMI-CONDUCTOR DEVICE, DIODE: SAME AS A066 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| -3 | \& CR13 <br>


\hline \& \& \& 59618140768 \& \& \& \& D \& A079 \& SEMI-CONDUCTOR DEVICE, DIODE: SAME AS A066 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| -3 | \& CR14 <br>


\hline \& \& \& 59618140768 \& \& \& \& D \& A080 \& SEMI-CONDUCTOR DEVICE, DIODE: SAME AS A066 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| :---: |
| $5-3$ | \& CR15 <br>

\hline
\end{tabular}



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\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{23}{|l|}{C3} \\
\hline \multicolumn{3}{|l|}{(1)} \& \multicolumn{7}{|r|}{REPAIRS PARTS FOR ON-SITE, AREA RESUPPLY,
AND DEPOT MAINTENANCE} \& \multirow[t]{4}{*}{\begin{tabular}{|c} 
(4) \\
U \\
N \\
1 \\
1 \\
T \\
OF \\
1 \\
I \\
S \\
S \\
U \\
\\
E
\end{tabular}} \& \multirow[t]{4}{*}{} \& \multirow[t]{4}{*}{\begin{tabular}{l}
(6) \\
QTY \\
INC IN UNIT
\end{tabular}} \& \multicolumn{3}{|l|}{\multirow[t]{3}{*}{\begin{tabular}{l}
(7) \\
(30 DAYS) SITE STOCKAGE ALLOWANCE
\end{tabular}}} \& \multicolumn{3}{|l|}{\multirow[t]{3}{*}{\begin{tabular}{l}
(8) \\
45 DAY AREA RESUPPLY ALLOW BASED ON NO. EQUIP. SUPPORTED
\end{tabular}}} \& \multirow[t]{4}{*}{(9)

1 YEAR
ALW
PER 100
EQUIP
CNTGCY

PLAN} \& \multirow[t]{4}{*}{} \& \multicolumn{2}{|l|}{\multirow[t]{2}{*}{| (11) |
| :--- |
| ILLUSTRATION |}} <br>

\hline \multirow[t]{3}{*}{} \& \multirow[t]{3}{*}{$$
\begin{aligned}
& \mathrm{M} \\
& \mathrm{~A} \\
& 1 \\
& \mathrm{~N} \\
& \mathrm{~N} \\
& \mathrm{D} \\
& \mathrm{D}
\end{aligned}
$$} \& \& (2) \& \& \& \& \& \& (3) \& \& \& \& \& \& \& \& \& \& \& \& \& <br>

\hline \& \& \& \& \multicolumn{3}{|r|}{MODEL} \& N \& \& \& \& \& \& \& \& \& \& \& \& \& \& (A) \& (B) <br>

\hline \& \& \& FEDERAL STOCK NUMBER \& 12 \& \& 56 \& D \& \& DESCRIPTION \& \& \& \& $$
\begin{gathered}
(\mathrm{A}) \\
1-5
\end{gathered}
$$ \& \[

$$
\begin{gathered}
(B) \\
6-10
\end{gathered}
$$

\] \& ${ }_{11-20}^{(C)}$ \& \[

$$
\begin{aligned}
& \text { (A) } \\
& 1-5
\end{aligned}
$$

\] \& \[

$$
\begin{array}{|c|c|}
(B) \\
6-10
\end{array}
$$
\] \& ${ }_{11-20}^{(C)}$ \& \& \& FIG.

NO. \&  <br>

\hline \& \& \& 59627911082 \& \& \& \& D \& A154 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& $\begin{array}{r}-15 \\ \hline-6 \\ \hline\end{array}$ \& Z12 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A155 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-6$ | \& Z17 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A156 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| -6 | \& Z18 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A157 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& $\begin{array}{r}-15 \\ \hline-6 \\ \hline\end{array}$ \& Z19 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A158 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-6$ | \& Z20 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A159 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& $\begin{array}{r}-15 \\ \hline-6-6 \\ \hline\end{array}$ \& Z25 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A160 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-6$ | \& Z26 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A161 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-6$ | \& Z27 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A162 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& $\begin{array}{r}-15 \\ \hline 5-6 \\ \hline\end{array}$ \& Z28 <br>


\hline P \& H \& T \& 74409594502 \& \& \& \& C \& A163 \& | CIRCUIT, CARD ASSEMBLY: |
| :--- |
| 58189; A52634-001 | \& EA \& \& 1 \& 1 \& 2 \& 3 \& 1 \& 2 \& 3 \& \& 3 \& \[

$$
\begin{aligned}
& -15 \\
& 4-2
\end{aligned}
$$
\] \& 7 <br>

\hline
\end{tabular}

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TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-21



\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{23}{|l|}{C3} \\
\hline \multicolumn{3}{|l|}{(1)} \& \multicolumn{7}{|r|}{REPAIRS PARTS FOR ON-SITE, AREA RESUPPLY,
AND DEPOT MAINTENANCE} \& \multirow[t]{4}{*}{\begin{tabular}{|c} 
(4) \\
U \\
N \\
N \\
I \\
OF \\
I \\
I \\
S \\
S \\
U \\
E
\end{tabular}} \& \multirow[t]{4}{*}{(5)

QTY
INC
IN
UNIT

PK} \& \multirow[t]{4}{*}{\begin{tabular}{l}
(6) <br>
QTY <br>
inc IN UNIT

} \& \multicolumn{3}{|l|}{\multirow[t]{3}{*}{

(7) <br>
(30 DAYS) SITE STOCKAGE ALLOWANCE

}} \& \multicolumn{3}{|l|}{\multirow[t]{3}{*}{

(8) <br>
45 DAY AREA RESUPPLY ALLOW BASED ON NO EQUIP. SUPPORTED
\end{tabular}}} \& \multirow[t]{4}{*}{(9)

$$
\begin{aligned}
& 1 \text { YEAR } \\
& \text { ALW } \\
& \text { PER } 100 \\
& \text { EQUIPP } \\
& \text { CNTGCY }
\end{aligned}
$$} \& \multirow[t]{4}{*}{\[

$$
\begin{gathered}
\hline \text { (10) } \\
\\
\\
\text { DEPOT } \\
\text { MANT } \\
\text { ALW } \\
\text { PER } \\
\text { 100 } \\
\text { EQUIP }
\end{gathered}
$$

\]} \& \multicolumn{2}{|l|}{\multirow[t]{2}{*}{| (11) |
| :--- |
| ILLUSTRATION |}} <br>

\hline \multirow[t]{3}{*}{$$
\begin{aligned}
& \text { (A) } \\
& \text { S } \\
& \text { O } \\
& \text { R } \\
& \text { C } \\
& \text { E } \\
& \text { C } \\
& \text { D }
\end{aligned}
$$} \& \multirow[t]{3}{*}{} \& \& (2) \& \& \& \& \& \& (3) \& \& \& \& \& \& \& \& \& \& \& \& \& <br>

\hline \& \& $$
\mathrm{c}
$$ \& \& \multicolumn{3}{|r|}{MODEL} \& I \& \& \& \& \& \& \& \& \& \& \& \& \& \& (A) \& (B) <br>

\hline \& \& $$
\begin{array}{|l}
\mathrm{C} \\
\mathrm{D} \\
\mathrm{D} \\
\mathrm{E}
\end{array}
$$ \& FEDERAL STOCK NUMBER \& 12 \& \& 56 \& D \& \& DESCRIPTION \& \& \& \& \[

$$
\begin{aligned}
& \text { (A) } \\
& 1-5
\end{aligned}
$$

\] \& \[

$$
\begin{array}{|c}
(B) \\
6-10
\end{array}
$$

\] \& (C) ${ }_{11-20}$ \& (A) \& \[

$$
\begin{array}{|c|c|}
(B) \\
6-10
\end{array}
$$
\] \& ${ }_{11-20}^{(C)}$ \& \& \& Fig.

NO. \&  <br>

\hline \multirow{10}{*}{P} \& \multirow{10}{*}{D} \& \& 59627911082 \& \& \& \& D \& A214 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| -7 | \& Z18 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A215 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-7$ | \& Z19 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A216 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& $\begin{array}{r}-15 \\ \hline-7 \\ \hline\end{array}$ \& Z22 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A217 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| -7 | \& Z23 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A218 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-7$ | \& Z26 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A219 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& $\begin{array}{r}-15 \\ \hline 5-7 \\ \hline\end{array}$ \& Z27 <br>


\hline \& \& \& 59627911082 \& \& \& \& D \& A220 \& | INTEGRATED CIRCUIT, LOGIC GATE: |
| :--- |
| SAME AS A020 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-7$ | \& Z28 <br>


\hline \& \& \& 59056832239 \& \& \& \& D \& A221 \& | RESISTOR, FIXED, COMPOSITION: |
| :--- |
| 81349; RC07GF201J | \& EA \& \& 3 \& \& \& \& \& \& \& \& 9 \& | -15 |
| :---: |
| $5-7$ | \& R1 <br>


\hline \& \& \& 59056832239 \& \& \& \& D \& A222 \& RESISTOR, FIXED, COMPOSITION: SAME AS A221 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| :---: |
| $5-7$ | \& R3 <br>

\hline \& \& \& 59056832239 \& \& \& \& D \& A223 \& RESISTOR, FIXED, COMPOSITION: SAME AS A221 \& EA \& \& REF \& \& \& \& \& \& \& \& \& $$
\begin{aligned}
& -15 \\
& 5-7
\end{aligned}
$$ \& R5 <br>

\hline
\end{tabular}





TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO31W4-2G-21



C3


C3





TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-21


| (4) | (5) |  |
| :---: | :---: | :---: |
| U |  |  |
| N |  |  |
| 1 |  |  |
| $T$ |  |  |
| OF |  |  |
| $I$ | QTY |  |
| S | INC |  |
| S | IN |  |
| U | UNIT |  |
| E | PK |  |



| (9) | (10) | (11) |  |
| :---: | :---: | :--- | :---: |
|  |  |  |  |
|  |  | ILLUSTRATION |  |
|  |  |  |  |
| 1 YEAR | DEPOT |  |  |
| ALW | MAINT | (A) | (B) |
| PER 100 | ALW |  | ITEM |
| EQUIP | PER |  | NO. |
| CNTGCY | 100 | FIG. | OR REF |
| PLAN | EQUIP | NO. | DESIGN |










| C3 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| C3 ${ }^{(1)}$ |  |  | REPAIRS PARTS FOR ON-SITE, AREA RESUPPLY,AND DEPOT MAINTENANCE |  |  |  |  |  |  | (4) <br> U <br> N <br> N <br> I <br> OF <br> I <br> I <br> S <br> S <br> U <br> E | $\begin{array}{\|c\|} \text { (5) } \\ \\ \\ \text { OTY } \\ \text { OTC } \\ \text { IN } \\ \text { INTT } \\ \text { UKI } \end{array}$ | (6) <br> QTY <br> inc IN UNIT | (7) <br> (30 DAYS) SITE STOCKAGE ALLOWANCE |  |  | (8) <br> 45 DAY AREA RESUPPLY ALLOW BASED ON NO EQUIP. SUPPORTED |  |  | (9) <br> 1 YEAR ALW PER 100 CNTGCY PLAN |  | (11) <br> ILLUSTRATION |  |
| (A) <br> S <br> O <br> U <br> R <br> C <br> E <br> C <br> C | $\left(\left.\begin{array}{l} \text { (B) } \\ M \\ A \\ A \\ 1 \\ N \\ T \\ D \\ C \end{array} \right\rvert\,\right.$ |  | (2) |  |  |  |  |  | (3) |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | MODEL |  |  | N |  |  |  |  |  |  |  |  | (A) | (B) |  |  |  |  |
|  |  |  | FEDERAL STOCK NUMBER | 12 |  | 5 | ${ }_{6}{ }^{\text {c }}$ D |  | DESCRIPTION |  |  |  | (A) | (B) | ${ }_{11-20}^{(C)}$ |  |  |  | (A) |  | $\begin{array}{\|c\|c\|} (B) \\ 6-10 \end{array}$ | ${ }_{11-20}^{(C)}$ | FIG. <br> No. |  |
| P | D |  | 59056869997 |  |  |  | D | A386 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A382 | EA |  | REF |  |  |  |  |  |  |  |  |  | -15 $5-11$ | R42 |
|  |  |  | 59056869997 |  |  |  | D | A387 | RESISTOR, FIXED, COMPOSITION: SAME AS A382 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r}-15 \\ 5-11 \\ \hline\end{array}$ | R52 |
|  |  |  | 59056869997 |  |  |  | D | A388 | RESISTOR, FIXED, COMPOSITION: SAME AS A382 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r}-15 \\ 5-11 \\ \hline\end{array}$ | R62 |
|  |  |  | 59056869997 |  |  |  | D | A389 | RESISTOR, FIXED, COMPOSITION: SAME AS A382 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r}-15 \\ 5-11 \\ \hline\end{array}$ | R72 |
|  |  |  | 59056869997 |  |  |  | D | A390 | RESISTOR, FD(ED, COMPOSITION: SAME AS A382 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r}-15 \\ \hline 5-11 \\ \hline\end{array}$ | R82 |
|  |  |  | 59058000179 |  |  |  | D | A391 | RESISTOR, FIXED, COMPOSITION: <br> 81349; RC07GF563J | EA |  | 10 |  |  |  |  |  |  |  | 30 | -15 <br> $5-11$ | R3 |
|  |  |  | 59058000179 |  |  |  | D | A392 | RESISTOR, FIXED, COMPOSITION: SAME AS A391 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-11$ | R13 |
|  |  |  | 59058000179 |  |  |  | D | A393 | RESISTOR, FIXED, COMPOSITION: SAME AS A391 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-11$ | R23 |
|  |  |  | 59058000179 |  |  |  | D | A394 | RESISTOR, FIXED, COMPOSITION: SAME AS A391 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r} -15 \\ 5-11 \\ \hline \end{array}$ | R33 |
|  |  |  | 59058000179 |  |  |  | D | A395 | RESISTOR, FIXED, COMPOSITION: SAME AS A391 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r} -15 \\ 5-11 \end{array}$ | R43 |




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\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{4}{*}{$$
\begin{array}{c|}
\hline(\mathrm{A}) \\
\mathrm{S} \\
\mathrm{O} \\
\mathrm{U} \\
\mathrm{R} \\
\mathrm{C} \\
\mathrm{E} \\
\mathrm{C} \\
\mathrm{D}
\end{array}
$$} \& \& \& \multicolumn{8}{|r|}{REPAIRS PARTS FOR ON-SITE, AREA RESUPPLY,
AND DEPOT MAINTENANCE} \& \multirow[t]{4}{*}{} \& \multirow[t]{4}{*}{(5)

QTY
INC
IN
UNIT

PK} \& \multirow[t]{4}{*}{} \& \multicolumn{3}{|l|}{\multirow[t]{3}{*}{\begin{tabular}{l}
(7) <br>
(30 DAYS) SITE STOCKAGE ALLOWANCE

}} \& \multicolumn{3}{|l|}{\multirow[t]{3}{*}{

(8) <br>
45 DAY AREA <br>
RESPPLY ALLOW <br>
BASED <br>
EQUPP. SUPPORTED
\end{tabular}}} \& \multirow[t]{4}{*}{(9)

1 YEAR
ALW
PER 100
EQUUP
CNTGCY

PLAN} \& \multirow[t]{4}{*}{\begin{tabular}{l}
(10) <br>
DEPOT MAINT ALW
PER 100 EQUIP

} \& \multicolumn{2}{|l|}{\multirow[t]{2}{*}{

(11) <br>
ILLUSTRATION
\end{tabular}}} <br>

\hline \& \& $$
\begin{aligned}
& \mathbf{R} \\
& \mathbf{E}
\end{aligned}
$$ \& \multirow[t]{3}{*}{(2)

FEDERAL
STOCK
STM STOCK NUMBER} \& \multicolumn{3}{|r|}{\multirow[b]{2}{*}{MODEL}} \& \multirow[b]{3}{*}{D} \& \& \& (3) \& \& \& \& \& \& \& \& \& \& \& \& \& <br>
\hline \& N \& c \& \& \& \& \& \& N \& \& \& \& \& \& \& \& \& \& \& \& \& \& (A) \& (B) <br>

\hline \& \& \& \& \& \& 45 \& \& C \& \& DESCRIPTION \& \& \& \& (A) \& (B) \& ${ }_{11-20}^{(C)}$ \& (A) \& $$
\mid
$$ \& ${ }_{11-20}^{(C)}$ \& \& \& FIG.

NO. \& $$
\begin{aligned}
& \text { ORREF } \\
& \text { OESIGN } \\
& \text { DESGN }
\end{aligned}
$$ <br>

\hline \multirow{10}{*}{P} \& \multicolumn{2}{|l|}{\multirow{10}{*}{D}} \& 69056832238 \& \& \& \& \& D \& A416 \& RESISTOR, FIXED, COMPOSITION: SAME AS A224 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-11$ | \& R84 <br>


\hline \& \& \& 59056832238 \& \& \& \& \& D \& A417 \& RESISTOR, FIXED, COMPOSITION: SAME AS A224 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| :---: |
| $5-11$ | \& R87 <br>


\hline \& \& \& 59056863903 \& \& \& \& \& D \& A418 \& | RESISTOR, FIXED, COMPOSITION: |
| :--- |
| 81349; RC07GF333J | \& EA \& \& 9 \& \& \& \& \& \& \& \& 27 \& -15

$5-11$ \& R5 <br>

\hline \& \& \& 59056863903 \& \& \& \& \& D \& A419 \& | RESISTOR, FIXED, COMPOSITION: |
| :--- |
| SAME AS A418 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& \[

$$
\begin{array}{r}
-15 \\
5-11
\end{array}
$$
\] \& R15 <br>

\hline \& \& \& 59056863903 \& \& \& \& \& D \& A420 \& | RESISTOR, FIXED, COMPOSITION: |
| :--- |
| SAME AS A418 | \& EA \& \& REF \& \& \& \& \& \& \& \& \& \[

$$
\begin{array}{r}
-15 \\
\hline 5-11 \\
\hline
\end{array}
$$
\] \& R25 <br>

\hline \& \& \& 59056863903 \& \& \& \& \& D \& A421 \& RESISTOR, FIXED, COMPOSITION: SAME AS A418 \& EA \& \& REF \& \& \& \& \& \& \& \& \& $$
\begin{array}{r}
-15 \\
5-11 \\
\hline
\end{array}
$$ \& R35 <br>

\hline \& \& \& 59056863903 \& \& \& \& \& D \& A422 \& RESISTOR, FIXED, COMPOSITION: SAME AS A418 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| :---: |
| $5-11$ | \& R45 <br>


\hline \& \& \& 59056863903 \& \& \& \& \& D \& A423 \& RESISTOR, FIXED, COMPOSITION: SAME AS A418 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-11$ | \& R55 <br>


\hline \& \& \& 59056863903 \& \& \& \& \& D \& A424 \& RESISTOR, FIXED, COMPOSITION: SAME AS A418 \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-11$ | \& R65 <br>

\hline \& \& \& 59056863903 \& \& \& \& \& D \& A425 \& RESISTOR, FIXED, COMPOSITION: SAME AS A418 \& EA \& \& REF \& \& \& \& \& \& \& \& \& $$
\begin{array}{r}
-15 \\
5-11
\end{array}
$$ \& R75 <br>

\hline
\end{tabular}

C3


C3

TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31


C3


C3


Q35

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Q35

C3


C3


Q35


REPAIRS PARTS FOR ON-SITE, AREA RESUPPLY
(2)


596

TRANSISTOR: SAME AS A349 TRANSISTOR: SAME AS A349 TRANSISTOR: SAME AS A349 RANSISTOR: TRANSISTOR: SAME AS A349 TRANSISTOR: SAME AS A349 TRANSISTOR: SAME AS A349 TRANSISTOR: SAME AS A349 TRANSISTOR: SAME AS A349 SAME AS A349

TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31
(6)


0023/T
TE STOCKAGE

$$
\begin{gathered}
45 \text { DAY AREA } \\
\text { RESUPPLY ALLOW }
\end{gathered}
$$

ALLOWANCE
BASED ON NO.

$$
\begin{aligned}
& \text { BASED ON NO. } \\
& \text { EQUIP. SUPPORTED }
\end{aligned}
$$

$$
\begin{array}{l|l}
\text { QTY } & \\
&
\end{array}
$$

| PK | UNIT | (A) <br> $1-5$ | (B) <br> $6-10$ | (C) <br> $11-20$ | (A) <br> $1-5$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | REF |  |  |  |  |


| A) | (B) |
| :--- | :--- |
| -5 | $6-1$ |


| (B) |
| :---: |
| $6-10$ |

$(C)$
$11-20$
$11-20$
-

C3


Q35

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| TM 11-7440-215-15/NAVSHIPS 096 |  |  |
| :---: | :---: | :---: |
| $(7)$ | $(8)$ | $(9)$ |

(6)

TRANSISTOR: SAME AS A349
TRANSISTOR:
SAME AS A349
TRANSISTOR: SAME AS A349 SAME AS A081 TRANSISTOR: SAME AS A081 SAME AS A081 TRANSISTOR: SAME AS A081 TRANSISTOR: SAME AS A081
TRANSISTOR: SAME AS A081 TRANSISTOR: TRANSISTOR: SAME AS A081 TRANSISTOR:
SAME AS A081

(5) QTY
INC
IN
UNIT

| (8) |  | (9) | (10) | (11) |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DAY AREA PLY ALLOW D ON NO. SUPPORTED |  | 1 YEAR ALW PER 100 EQUIP CNTGCY PLAN | $\begin{gathered} \text { DEPOT } \\ \text { MAINT } \\ \text { ALW } \\ \text { PER } \\ \text { 100 } \\ \text { EQUIP } \end{gathered}$ | ILLUSTRATION |  |
|  |  | (A) |  | (B) |
|  |  |  |  | ITEM |
|  |  |  |  |  | NO. |
| (B) | (C) |  |  | FIG. | OR REF |
| 6-10 | 11-20 |  |  | NO. | DESIGN |
|  |  |  |  |  | -15 |  |



Q35

C3


TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31

Q35

C3


Q35


Q35

TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31


Q35

C3


C3


C3


Q35

C3


Q35

C3


TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31


Q35

C3


TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31

Q35

C3



C3


C3


Q35


C3


Q35


C3


Q35


Q35

TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31


Q35




Q35


C3


Q35



Q35

C3


Q35

C3



C3



C3


Change 388


C3


C3







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TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31



C3



C3





C3


C3


C3


C3


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TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31


Change 8114






C3


TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31


Change 5121

TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31


Change 3122

C3


TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31



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TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31


TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31


Q35


Q35

TM 11-7440-215-15/NAVSHIPS 0967-324-0023/TO 31W4-2G-31



Q35

C3

| C3 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | REPAIRS PARTS FOR ON-SITE, AREA RESUPPLY,AND DEPOT MAINTENANCE |  |  |  |  |  |  | (4) <br> U <br> N <br> 1 <br> $T$ <br> OF <br> 1 <br> S <br> S <br> S <br> U <br>  | $\begin{array}{\|l\|} \hline \text { (5) } \\ \\ \text { OTY } \\ \text { OTY } \\ \text { INC } \\ \text { IN } \\ \text { UNT } \\ \text { PK } \end{array}$ | (6) <br> QTY INC IN UNIT | (7) <br> (30 DAYS) SITE STOCKAGE ALLOWANCE |  |  | (8)45 DAY AREARESUPPLY ALLOWBASED NONEQUP. SUPPORTED |  |  |  |  | (11) <br> ILLUSTRATION |  |
|  |  |  | (2) <br> FEDERAL STOCK NUMBER |  |  |  |  |  | (3) |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | MODEL | $\stackrel{\text { I }}{ }$ |  |  | (A) | (B) |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | 12 | 34 | 56 | C |  | DESCRIPTION | (A) |  |  |  | (B) | ${ }_{11-20}^{(C)}$ | (A) | $\left\lvert\, \begin{array}{\|l\|l\|} \hline(\mathrm{B}) \\ 6-10 \end{array}\right.$ | (C) | FIG. NO. |  |  | $\begin{aligned} & \text { ORREF REF } \\ & \text { DESIG } \end{aligned}$ |
| P | H |  |  | 30309335356 |  |  |  | D | B205AI | AM BELT, POSITIVE DRIVE: 21678; 110XL037 | EA |  | 1 | 2 | 3 | 4 | 2 | 3 | 4 |  | 2 | -15 <br> $4-7$ | 66 |
| P | H |  |  | 30309428532 |  |  |  | D | B206AI | AM BELT, POSITIVE DRIVE: 21678; 260XL037 | EA |  | 1 | 2 | 3 | 4 | 2 | 3 | 4 |  | 2 | -15 <br> $4-7$ | 65 |
| X2 | H |  |  |  |  |  | D | B207 | BRACKET, CONNECTOR: 07264; C14563 | EA |  | 1 |  |  |  |  |  |  |  |  | -15 <br> $4-7$ | 237 |
|  |  |  | 53050546670 |  |  |  | * | B208 | SCREW, MACHINE: SAME AS A914 | EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $4-7$ | 235 |
|  |  |  | 53100541830 |  |  |  | * | B209 | WASHER, LOCK: SAME AS A894 | EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $4-7$ | 236 |
| X2 | H |  | 74409333660 |  |  |  | D | B210 | BUMPER, CARD: <br> 34631; 110653901 | EA |  | 1 |  |  |  |  |  |  |  |  | -15 <br> $4-7$ | 262 |
|  |  |  | 53050546670 |  |  |  | * | B211 | SCREW, MACHINE: SAME AS A914 | EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $4-7$ | 259 |
|  |  |  | 53108805978 |  |  |  | * | B212 | WASHER, FLAT: SAME AS A915 | EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $4-7$ | 261 |
|  |  |  | 53100541830 |  |  |  | * | B213 | WASHER, LOCK: SAME AS A894 | EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $4-7$ | 260 |
| C | H |  | 47309158176 |  |  |  | D | B214 | FITTING, HOSE: 30327; KA06-04MB | EA |  | 2 |  |  |  |  |  |  |  |  | -15 <br> $4-7$ | 8 |

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Q35


Q35

C3


Q35


Q35

C3


Q35


Q35

C3


Q35

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Change 8143

C3


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| (A) (B) ${ }^{(\text {B }}$ (C) |  |  | REPAIRS PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  | $\begin{array}{\|l\|} \hline \text { (6) } \\ \\ \text { OTY } \\ \text { ONY } \\ \text { INC } \\ \text { INIT } \end{array}$ | $\begin{gathered} \text { (7) } \\ \text { (30DAYS } \\ \text { SIESTOCKAGE } \\ \text { ALLOWANCE } \end{gathered}$ |  |  | (8) <br> 45 DAY AREA RESUPPLY ALLOW EQUIP. SUPPORTED |  |  | (9) <br> 1 YEAR PER 100 EQUIP PLAN | $\begin{gathered} \text { (10) } \\ \\ \text { DEPOT } \\ \text { MAINT } \\ \text { ALW } \\ \text { PER } \\ 100 \\ \text { EQUIP } \end{gathered}$ | (11) <br> illustration |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| U | $\left\|\begin{array}{l} \mathrm{A} \\ 1 \\ 1 \\ \mathrm{~N} \\ \mathrm{~d} \\ \mathrm{~d} \end{array}\right\|$ |  |  |  |  |  | FOR ON-SITE, AREA RESUPPLY EPOT MAINTENANCE <br> (3) <br> DESCRIPTION |  | $\underset{0}{1}$ |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  | $\left\lvert\, \begin{gathered} \text { of } \\ 1 \\ s \end{gathered}\right.$ |  |  |  |  |  | (A) | ${ }_{\text {ITEM }}^{\text {(B) }}$ |  |  |  |  |
|  |  |  |  | 1233456 D |  |  | $\underset{\mathrm{E}}{\mathrm{U}}$ | (A) | (B) |  |  | (C) | ( ${ }_{\text {( }}$ | (8) |  |  |  | (C) |  | Fig. | (tar |
| P | D |  | 59059529230 |  |  |  |  |  | D | B349A RESISTOR, FIXED, FILM: 81349; RN60D7500F | EA |  | 2 |  |  |  |  |  |  |  |  | 6 | -15 $5-16$ | R13 |
|  |  |  | 59059529230 |  |  |  | D | B350A RESISTOR, FIXED, FILM: SAME AS B349A | EA |  | REF |  |  |  |  |  |  |  |  | -15 | R28 |
| P P | D |  | 59051923973 |  |  |  | D | B351AM RESISTOR, FIXED, COMPOSITION: 81349; RC20GF471J | EA |  | 5 |  |  |  |  |  |  |  | 15 | -15 $5-16$ | R21 |
| P | D |  | 59052494195 |  |  |  | D | B352 M RESISTOR, FIXED, COMPOSITION: 81349; RC20GF752J | EA |  | 2 |  |  |  |  |  |  |  | 6 | -15 $5-16$ | R27 |
|  |  |  | 59051956806 |  |  |  | D | B353A RESISTOR, FIXED, COMPOSITION: <br> SAME AS B302A | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-16$ | R14 |
|  |  |  | 59051956806 |  |  |  | D | B354A RESISTOR, FIXED, COMPOSITION: <br> SAME AS B302A | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-16$ | R29 |
|  |  |  | 59050693914 |  |  |  | D | B355A RESISTOR, FIXED, FILM: SAME AS B307A | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r} -15 \\ \hline 5-16 \\ \hline \end{array}$ | R30 |
|  |  |  | 59051712006 |  |  |  | D | B356 M RESISTOR, FIXED, COMPOSITION: SAME AS B342B | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r} -15 \\ \hline 5-16 \\ \hline \end{array}$ | R19 |
|  |  |  | 59051712006 |  |  |  | D | B357 M RESISTOR, FIXED, COMPOSITION: SAME AS B342B | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r} -15 \\ 5-16 \\ \hline \end{array}$ | R34 |
| P | D |  | 59059841465 |  |  |  | D | B358A RESISTOR, FIXED, FILM: 81349; RN60D 5621F | EA |  | 5 |  |  |  |  |  |  |  | 15 | $\begin{array}{r} -15 \\ 5-16 \end{array}$ | R9 |

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\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{4}{*}{$$
\begin{array}{|c}
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$$} \& \& \& \multicolumn{6}{|r|}{REPAIRS PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE} \& \multirow[t]{4}{*}{$$
\begin{array}{|c|c|}
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QTY INC IN UNIT

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(7) <br>
(30 DAYS) SITE STOCKAGE ALLOWANCE
\end{tabular}}} \& \multicolumn{3}{|l|}{\multirow[t]{3}{*}{(8)

45 DAY AREA
RESUPPLY ALLOW
BASED NON

EQUP. SUPPORTED}} \& \multirow[t]{4}{*}{| (9) |
| :--- |
| 1 YEAR ALW PER 100 EQUIP CNTGCY PLAN |} \& \multirow[t]{4}{*}{\[

$$
\begin{gathered}
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\\
\text { DEPOT } \\
\text { MANT } \\
\text { ALW } \\
\text { PRR } \\
100 \\
\text { EQUIIP }
\end{gathered}
$$

\]} \& \multicolumn{2}{|l|}{\multirow[t]{2}{*}{| (11) |
| :--- |
| ILLUSTRATION |}} <br>

\hline \& \multicolumn{2}{|l|}{\multirow[t]{3}{*}{}} \& (2) \& \multicolumn{3}{|r|}{\multirow[b]{2}{*}{MODEL}} \& \& \multirow[t]{3}{*}{(3) ${ }_{\text {(3) }}$ DESCRIPTION} \& \& \& \& \& \& \& \& \& \& \& \& \& <br>

\hline \& \& \& \& \& \& \& \multirow[t]{2}{*}{$$
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& \mathrm{N} \\
& \mathrm{D} \\
& \mathrm{C} \\
& \mathrm{D}
\end{aligned}
$$} \& \& \& \& \& \& \& \& \& \& \& \& \& (A) \& (B) <br>

\hline \& \& \& \[
$$
\begin{aligned}
& \text { STOCK } \\
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$$

\] \& 12 \& \multicolumn{2}{|l|}{| 2 | 3 | 4 | 5 | 6 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |} \& \& \& \& \& \& (A) \& (B) \& ${ }_{11-20}^{(C)}$ \& (A) \& (B) \& ${ }_{11-20}^{(C)}$ \& \& \& FIG. \& \[

$$
\begin{aligned}
& \text { OR REF } \\
& \text { DESIGN }
\end{aligned}
$$
\] <br>

\hline \multirow{4}{*}{P} \& \& \& 59052793517 \& \& \& \& D \& | B359A RESISTOR, FIXED, COMPOSITION: |
| :--- |
| SAME AS B304A | \& EA \& \& REF \& \& \& \& \& \& \& \& \& $\begin{array}{r}-15 \\ 5-16 \\ \hline\end{array}$ \& R20 <br>

\hline \& D \& \& 59050518003 \& \& \& \& D \& B360A RESISTOR, FIXED, FILM: 81349; RN60D1582F \& EA \& \& 2 \& \& \& \& \& \& \& \& 6 \& -15
$5-16$ \& R25 <br>

\hline \& \& \& $$
\begin{aligned}
& 5905-00- \\
& 107-0818
\end{aligned}
$$ \& \& \& \& D \& B361A RESISTOR, VARIABLE: SAME AS B316AM \& EA \& \& REF \& \& \& \& \& \& \& \& \& -15

$5-16$ \& R17 <br>

\hline \& \& \& $$
\begin{aligned}
& 5905-00- \\
& 107-0818
\end{aligned}
$$ \& \& \& \& D \& B362A RESISTOR, VARIABLE: SAME AS B316AM \& EA \& \& REF \& \& \& \& \& \& \& \& \& $\begin{array}{r}-15 \\ \hline 5-16 \\ \hline\end{array}$ \& R32 <br>

\hline \multirow[t]{5}{*}{P} \& D \& \& 59059855435 \& \& \& \& D \& B363A RESISTOR, FIXED, FILM:

81349; RN60D7501F \& EA \& \& 1 \& \& \& \& \& \& \& \& 3 \& $$
\begin{array}{r}
-15 \\
5-16 \\
\hline
\end{array}
$$ \& R10 <br>

\hline \& \& \& 59059570643 \& \& \& \& D \& B364A RESISTOR, FIXED, FILM: SAME AS B314 M \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-16$ | \& R1 <br>


\hline \& \& \& 59059570643 \& \& \& \& D \& B365A RESISTOR, FIXED, FILM: SAME AS B314 M \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-16$ | \& R2 <br>


\hline \& \& \& 59059570643 \& \& \& \& D \& B366 M RESISTOR, FIXED, FILM: SAME AS B314 M \& EA \& \& REF \& \& \& \& \& \& \& \& \& | -15 |
| ---: |
| $5-16$ | \& R3 <br>

\hline \& \& \& 59059570643 \& \& \& \& D \& B367 M RESISTOR, FIXED, FILM: SAME AS B314 M \& EA \& \& REF \& \& \& \& \& \& \& \& \& $$
\begin{array}{r}
-15 \\
5-16 \\
\hline
\end{array}
$$ \& R23 <br>

\hline \multirow[t]{2}{*}{P} \& \multirow[t]{2}{*}{D} \& \& 59055429387 \& \& \& \& D \& | B368A RESISTOR, FIXED, WIREWOUND: |
| :--- |
| 81349; RW59V102 | \& EA \& \& 1 \& \& \& \& \& \& \& \& 6 \& \[

$$
\begin{array}{r}
-15 \\
5-16 \\
\hline
\end{array}
$$
\] \& R24 <br>

\hline \& \& \& 59055429387 \& \& \& \& D \& | B369A RESISTOR, FIXED, WIREWOUND: |
| :--- |
| SAME AS B368A | \& EA \& \& REF \& \& \& \& \& \& \& \& \& \[

$$
\begin{array}{r}
-15 \\
5-16
\end{array}
$$
\] \& R26 <br>

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\end{tabular}



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C3

|  |  |  | REPAIRS PARTS FOR ON-SITE, AREA RESUPPLY,AND DEPOT MAINTÉNANCE |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | (2) |  |  |  |  |  | (3) |
|  |  |  | MODEL |  |  |
|  |  |  | FEDERAL STOCK NUMBER |  | 12 | 3 | 45 | 6 | DESCRIPTION |
| P | D |  |  | 59108388395 |  |  |  |  | E |  |
|  |  |  | 59108388395 |  |  |  |  | E | B823 CAPACITOR, FIXED, PAPER: <br> SAME AS B465 M |
|  |  |  | 59108388395 |  |  |  |  | E | B824 CAPACITOR, FIXED, PAPER: <br> SAME AS B465 M |
|  |  |  | 59108388395 |  |  |  |  | E | B825 CAPACITOR, FIXED, PAPER: <br> SAME AS 8465 M |
|  |  |  | 59055780997 |  |  |  |  | E | B826 RESISTOR, FIXED, WIREWOUND: <br> SAME AS B417A |
|  |  |  | 59058434711 |  |  |  |  | E | B827A RESISTOR, FIXED, WIREWOUND: <br> 81349; RW59V1RS |
|  |  |  | 59051956791 |  |  |  |  | E | B828ARESISTOR, FIXED, COMPOSITION: <br> SAME AS B413 M |
|  |  |  | 59051712006 |  |  |  |  | E | B829A RESISTOR, FIXED, COMPOSITION: SAME AS B342B |
|  |  |  | 59051908889 |  |  |  |  | E | B830B RESISTOR, FIXED, COMPOSITION: <br> SAME AS A340 |
|  |  |  | 59051712006 |  |  |  |  | E | B831A RESISTOR, FIXED, COMPOSITION: <br> SAME AS 8342B |

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| (4)UNI$T$OF1$S$$S$$U$$U$E |  | (6) | (7) <br> (30 DAYS) SITE STOCKAGE ALLOWANCE |  |  | (8) <br> 45 DAY AREA RESUPPLY ALLOW BASED ON NO. EQUIP. SUPPORTED |  |  | (9) <br> 1 YEAR PER 100 EQUIP CNTGCY PLAN | (10)$\begin{gathered} \text { DEPOT } \\ \text { MAINT } \\ \text { ALW } \\ \text { PER } \\ \text { 100 } \\ \text { EQUIP } \\ \hline \end{gathered}$ | (11) <br> ILLUSTRATION |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  | (A) | (B) |  |  |
|  |  |  | (A) | (B) | $\begin{gathered} (\mathrm{C}) \\ 11-20 \end{gathered}$ |  |  |  | (A) |  | $\begin{gathered} \text { (B) } \\ 6-10 \end{gathered}$ | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ | FIG. NO. | $\begin{aligned} & \text { ORU. } \\ & \text { OR REF } \\ & \text { DESIGN } \end{aligned}$ |
| EA |  | REF |  |  |  |  |  |  |  |  |  | -15 | C2 |
| EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r} -15 \\ 5-228 \end{array}$ | C3 |
| EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r} -15 \\ \hline 5-22 \mathrm{~B} \\ \hline \end{array}$ | C4 |
| EA |  | REF |  |  |  |  |  |  |  |  | -15 | C5 |
| EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $5-22 B$ | R1 |
| EA |  | 1 |  |  |  |  |  |  |  | 3 | -15 <br> $5-22 B$ | R2 |
| EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $5-22 B$ | R3 |
| EA |  | REF |  |  |  |  |  |  |  |  | -15 | R4 |
| EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $5-22 B$ | R8 |
| EA |  | REF |  |  |  |  |  |  |  |  | -15 <br> $5-22 B$ | R6 |

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Change 8 I-3 (I-4 Blank)

By Order of the Secretaries of the Army, the Navy, and the Air Force:

Official:
VERNE L. BOWERS,
Major General, United States Army, The Adjutant General.
W. C. WESTMORELAND, General, United States Army, Chief of Staff.

JOSEPH E. RICE,
Rear Admiral, U.S. Navy, Commander Naval Electronics Systems Command.

## Official:

JOHN D. RYAN, General, USAF, Chief of Staff.
DWIGHT W. COVELL, Colonel, USAF, Director of Administration.

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CNGB (1)
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USASESS (5)
USAINTS (3)
USASCS (6)
7th \& 8th Armies (4)
Corps (2)
$N G:$ None
USAR: None
For explanation of abbreviations used, see AR 810-50.

Sig Bde (USASTRATCOM) Korea (3)
Sig Gp (USASTRATCOM) Japan (3)
Sig Gp (USASTRATCOM) Taiwan (3)
Army Depots (2) except
ARAD (10)
LBAD (10)
SAAD (25)
TOAD (14)
Gen Deps (2) except
Pirmasens (10)
Sig Dep (4)
Sig Sec Gen Deps (4)
Sig FLDMS (1)
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11-867
11-868
11-500 (AA-AC)
29-134
29-136


# The Metric System and Equivalents 

## Linear Measure

1 centimeter $=10$ millimeters $=.39$ inch 1 decimeter $=10$ centimeters $=3.94$ inches 1 meter $=10$ decimeters $=39.37$ inches 1 dekameter $=10$ meters $=32.8$ feet 1 hectometer $=10$ dekameters $=328.08$ feet 1 kilometer $=10$ hectometers $=3,280.8$ feet

## Weights

1 centigram = 10 milligrams $=.15$ grain 1 decigram $=10$ centigrams $=1.54$ grains 1 gram = 10 decigram = .035 ounce 1 decagram $=10$ grams $=.35$ ounce
1 hectogram = 10 decagrams = 3.52 ounces
1 kilogram $=10$ hectograms $=2.2$ pounds
1 quintal $=100$ kilograms $=220.46$ pounds
1 metric ton $=10$ quintals $=1.1$ short tons

## Liquid Measure

$$
\begin{aligned}
& 1 \text { centiliter = } 10 \text { milliters = } .34 \text { fl. ounce } \\
& 1 \text { deciliter }=10 \text { centiliters }=3.38 \text { fl. ounces } \\
& 1 \text { liter }=10 \text { deciliters }=33.81 \text { fl. ounces } \\
& 1 \text { dekaliter }=10 \text { liters }=2.64 \text { gallons } \\
& 1 \text { hectoliter }=10 \text { dekaliters }=26.42 \text { gallons } \\
& 1 \text { kiloliter }=10 \text { hectoliters }=264.18 \text { gallons }
\end{aligned}
$$

## Square Measure

1 sq. centimeter $=100$ sq. millimeters $=.155$ sq. inch
1 sq. decimeter $=100$ sq. centimeters $=15.5$ sq. inches
1 sq. meter $($ centare $)=100$ sq. decimeters $=10.76$ sq. feet
1 sq. dekameter $($ are $)=100$ sq. meters $=1,076.4$ sq. feet
1 sq. hectometer (hectare) $=100$ sq. dekameters $=2.47$ acres
1 sq. kilomete $=100$ sq. hectometers $=.386$ sq. mile

Cubic Measure

1 cu . centimeter $=1000 \mathrm{cu}$. millimeters $=.06 \mathrm{cu}$. inch
1 cu . decimeter $=1000 \mathrm{cu}$. centimeters $=61.02 \mathrm{cu}$. inches
1 cu . meter $=1000 \mathrm{cu}$. decimeters $=35.31 \mathrm{cu}$. feet

## Approximate Conversion Factors

| To change | To | Multiply by | To change | To | Multiply by |
| :---: | :---: | :---: | :---: | :---: | :---: |
| inches | centimeters | 2.540 | ounce-inches | Newton-meters | . 007062 |
| feet | meters | . 305 | centimeters | inches | . 394 |
| yards | meters | . 914 | meters | feet | 3.280 |
| miles | kilometers | 1.609 | meters | yards | 1.094 |
| square inches | square centimeters | 6.451 | kilometers | miles | . 621 |
| square feet | square meters | . 093 | square centimeters | square inches | . 155 |
| square yards | square meters | . 836 | square meters | square feet | 10.764 |
| square miles | square kilometers | 2.590 | square meters | square yards | 1.196 |
| acres | square hectometers | . 405 | square kilometers | square miles | . 386 |
| cubic feet | cubic meters | . 028 | square hectometers | acres | 2.471 |
| cubic yards | cubic meters | . 765 | cubic meters | cubic feet | 35.315 |
| fluid ounces | milliliters | 29,573 | cubic meters | cubic yards | 1.308 |
| pints | liters | . 473 | milliliters | fluid ounces | . 034 |
| quarts | liters | . 946 | liters | pints | 2.113 |
| gallons | liters | 3.785 | liters | quarts | 1.057 |
| ounces | grams | 28.349 | liters | gallons | . 264 |
| pounds | kilograms | . 454 | grams | ounces | . 035 |
| short tons | metric tons | . 907 | kilograms | pounds | 2.205 |
| pound-feet | Newton-meters | 1.356 | metric tons | short tons | 1.102 |
| pound-inches | Newton-meters | . 11296 |  |  |  |

## Temperature (Exact)

| ${ }^{\circ} \mathrm{F}$ | Fahrenheit | 5/9 (after | Celsius | ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :--- | :--- | :--- |
|  | temperature | subtracting 32) | temperature |  |

PIN: 011152-000


[^0]:    -- ELECTRICAL SIGNALS

    - CARD FLOW
    -     -         - MECHANICAL POWER DISTRIBUTION
    -.-.- SOLENOID ACTION
    = AIR FLOW ACTION

